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INTERNATIONAL EDITION
MARCH 17, 1988

EDN®

Part 2 of EDN's Decade 90 Series

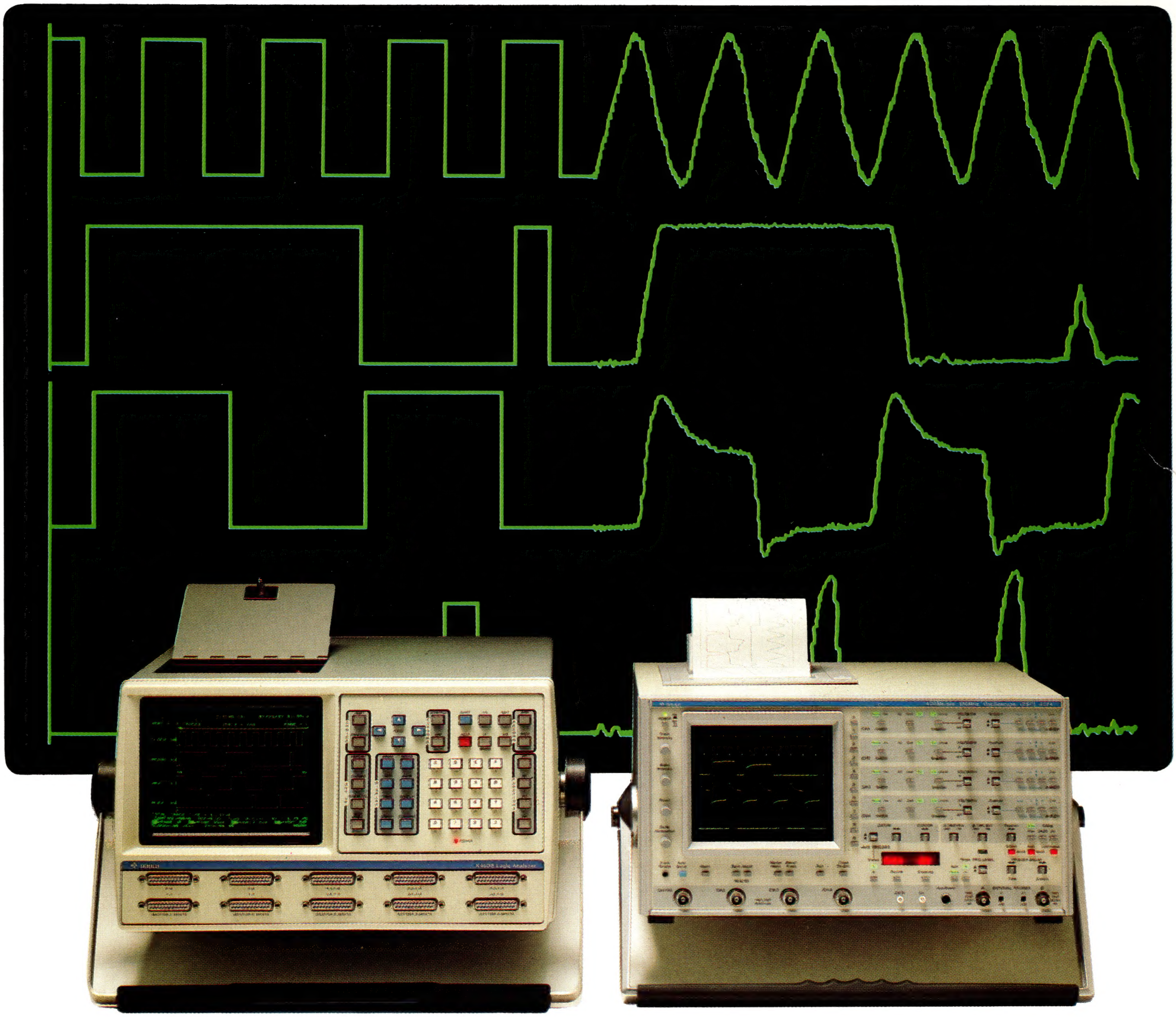
Design crystal oscillators with wide tuning range

Monolithic filters for data-acquisition systems

Update on CASE

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Viable VGA-emulator chip sets reach design marketplace



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Circle No. 6 for K450B, Circle No. 45 for 4074

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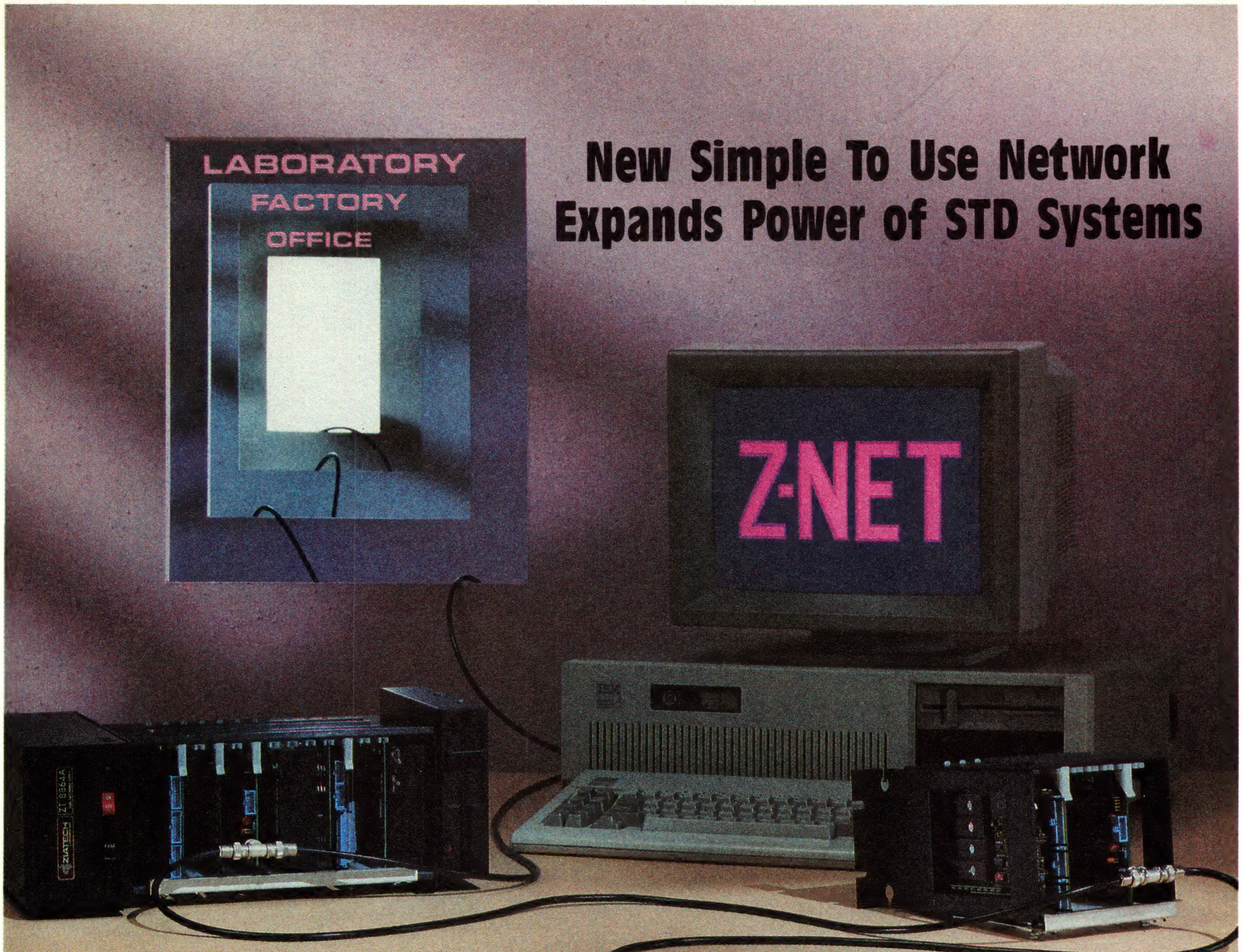
Electronics

New Simple To Use Network Expands Power of STD Systems



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Circle No 4

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And the only one that's designed specifically to operate with 8-bit flash converters.

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The VA730 Sample & Hold Amp is just part of VTC's broad line of Linear Signal Processing (LSP) ICs, which includes *Op Amps* to 500MHz gain bandwidth . . . precision, high-speed, and fast settling, plus dual and quad . . . with no sacrifice in performance.

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DACs to 12 bits, 100nsec settling time.

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Most of these standard parts are also available as cells in our 6GHz Linear/Digital Bipolar Standard Cell Library, the VL3000.

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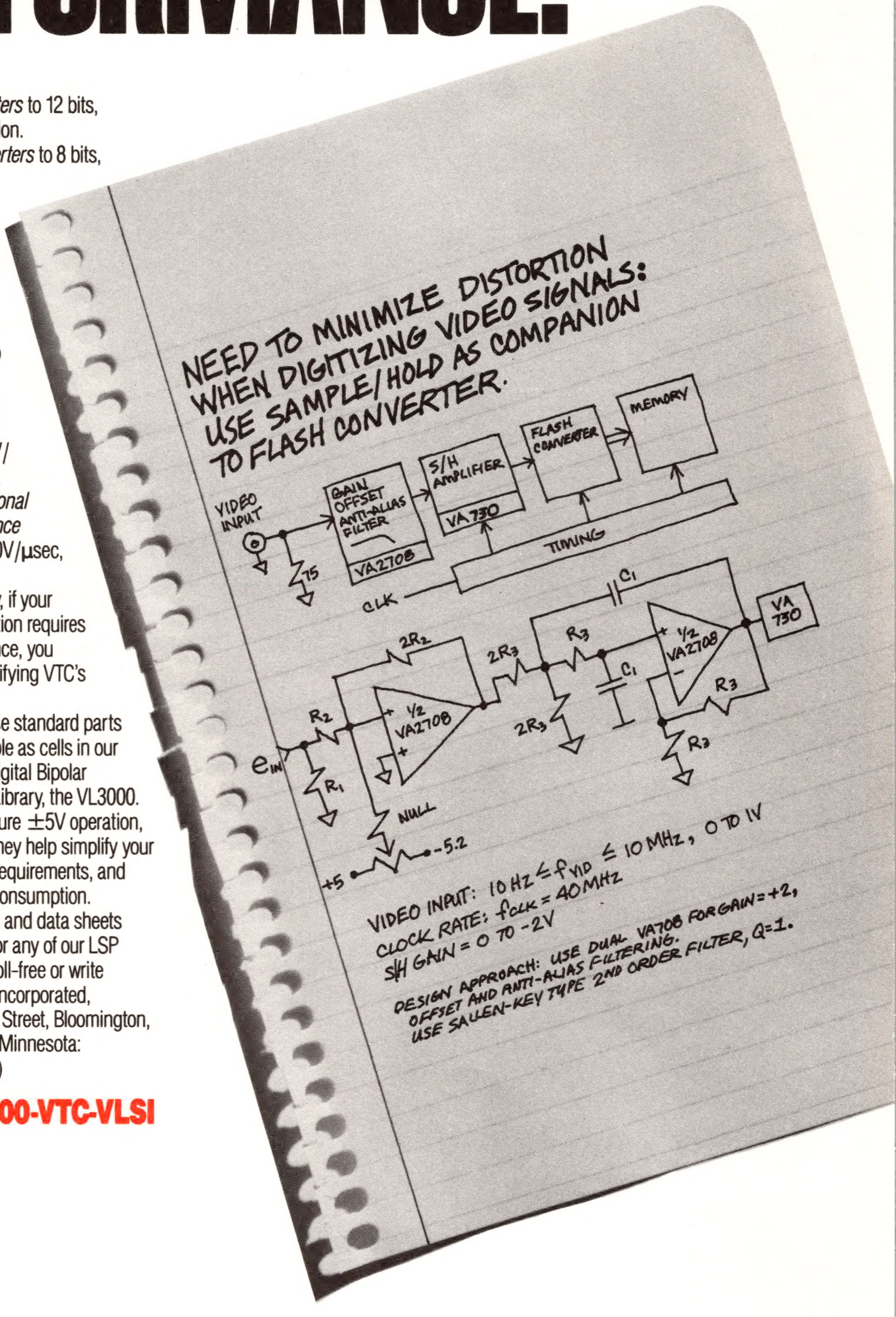
CALL 1-800-VTC-VLSI



NEED TO MINIMIZE DISTORTION WHEN DIGITIZING VIDEO SIGNALS: USE SAMPLE/HOLD AS COMPANION TO FLASH CONVERTER.

VIDEO INPUT: $10\,\text{HZ} \le f_{VID} \le 10\,\text{MHz}$, 0 TO 1V
CLOCK RATE: $f_{CLK} = 40\,\text{MHz}$
S/H GAIN = 0 TO -2V

DESIGN APPROACH: USE DUAL VA708 FOR GAIN=+2, OFFSET AND ANTI-ALIAS FILTERING.
USE SALLEN-KEY TYPE 2ND ORDER FILTER, Q=1.

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Circle No 5

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Starting now, that's how it'll be, if you have our new WaveTest® software.

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92138. TWX 910-335-2007.

Circle 1 for Literature

Circle 40 for Demonstration

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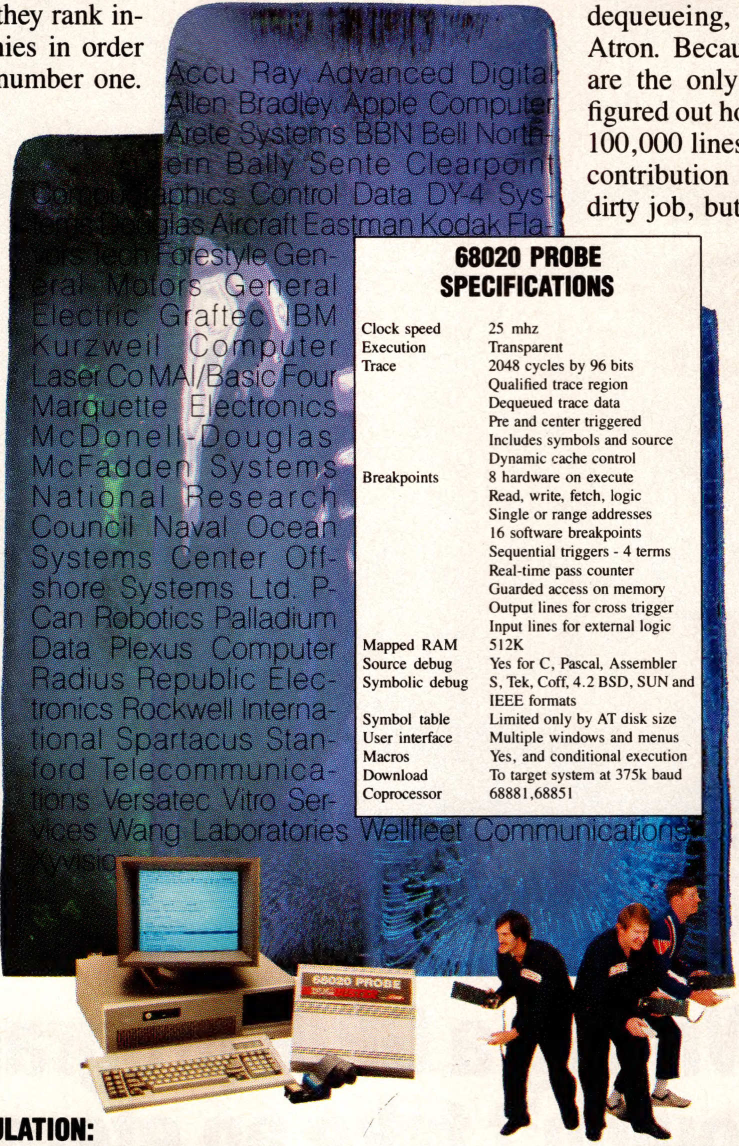
WHO YA GONNA CALL TO ICE 68020 BUGS? ATRON BUGBUSTERS!

We recently received a competitive analysis written by a billion-dollar competitor of ours. In it, they rank in-circuit emulation companies in order of importance. We were number one.

SO WHO'S ATRON?

Today, Atron is the number-one supplier of hardware-assisted software debuggers for 8088/80286/80386-based PCs. Nine of the top ten software packages were written by Atron customers. Everybody from AST to Borland to Oracle to Zenith. Now, we can make the same claim in the 68020 marketplace.

Everybody from Apple (MAC IIs) to Wellfleet (datacom) will attest to the superiority of Atron's 68020 debugging technology. One Atron customer even said, "We sent our non-Atron ICE unit out several months ago for repairs; nobody around here seems to know or care if it's back yet. The Atron unit is the tool of choice."



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68020 PROBE SPECIFICATIONS

Clock speed	25 mhz
Execution	Transparent
Trace	2048 cycles by 96 bits Qualified trace region Dequeued trace data Pre and center triggered Includes symbols and source Dynamic cache control
Breakpoints	8 hardware on execute Read, write, fetch, logic Single or range addresses 16 software breakpoints Sequential triggers - 4 terms Real-time pass counter Guarded access on memory Output lines for cross trigger Input lines for external logic
Mapped RAM	512K
Source debug	Yes for C, Pascal, Assembler
Symbolic debug	S, Tek, Coff, 4.2 BSD, SUN and IEEE formats
Symbol table	Limited only by AT disk size
User interface	Multiple windows and menus
Macros	Yes, and conditional execution
Download	To target system at 375k baud
Coprocessor	68881,68851

25-MHZ, REAL-TIME, EMULATION: SOONER OR LATER, YOU KNOW YOU'LL NEED IT.

Why invest in a slower emulator (especially one that costs more)? Some bugs only occur in real time, and you know your next design will be 25 mhz. Before Atron's state-of-the-art design, there was no such thing as a 25-mhz emulator. There still isn't another one anywhere near our price.

PROBE CAN TRACE IT THROUGH THE PIPELINE, SO YOU WON'T LOSE YOUR MIND.

The 68020 has an on-board pre-fetch pipeline. Without Atron's 68020 PROBE, your best software engineer will spend a lot of time figuring out which instructions actually execute, and then, which bus cycles go with those instructions. The 68020 PROBE eliminates all these tedious mental translations and displays what the processor really did. The technology, called pipeline dequeueing, is only available from Atron. Because the Atron bugbusters are the only ones anywhere who've figured out how to do it. And it took us 100,000 lines of code. Consider it our contribution to your sanity. (It was a dirty job, but somebody had to do it.)

LET THE SOURCE BE WITH YOU.

Why spend all day doing mental translations between your C source code and the machine code in your target? These tedious operations are eliminated with Atron's source-level debugging capabilities.

Since PROBE uses a PC AT as its instrumentation chassis, you can get compiled code to its target via Ethernet, VAXNet, SUNNet, SCSI or RS-232. And whether you are compiling on a PC, a workstation or a VAX, Atron supports more object-module formats than anybody else (see specification box).

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☐ Please send me your 36-page 68020 PROBE user's guide, with its command summary and examples of use.

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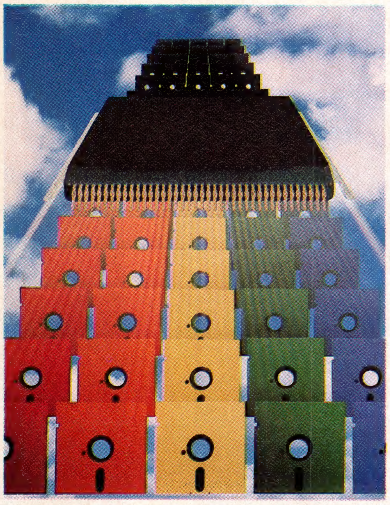
Volume 33, Number 6

EDN

March 17, 1988

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *VGA chip sets bring color graphics within designers' reach. See pg 118. (Photo courtesy Video Seven Inc)*

DESIGN FEATURES

Special Report: VGA chip sets 118

While debating degrees of compatibility with IBM's Video Graphics Array standard, manufacturers of VGA-like chips are attempting to woo designers by offering exotic features and backward compatibility with other IBM display products.—*J D Mosley, Regional Editor*

Decade 90: The future of system design—Part 2 130

The next decade's billion-transistor ICs will rapidly make manual system-design methods obsolete. If engineers are to tackle larger, more complex electronic designs, they will need automated design tools. Today's CAE tools help engineers develop system components. Tomorrow's tools will help designers develop entire systems.—*Steven H Leibson, Regional Editor*

Design method yields low-noise, wide-range crystal oscillators 141

A characterization technique allows you to design frequency-determining networks for tunable crystal oscillators.—*Tim L Hillstrom, Hewlett-Packard Co*

System architecture dominates design of no-wait-state cache 155

To extract maximum efficiency from today's 32-bit CPUs, you must provide them with zero-wait-state access to program and data memory. —*James K Flynn and Narciso Mera, AT&T Microelectronics*

Token-bus-controller interface must resolve family disparities 167

A system designed for a token bus network can benefit from a token bus controller such as the MC68824. The amount of glue logic required to interface the host to the controller will differ, however.—*Paul Polansky, Motorola Inc*

Evaluate model types before simulating logic circuits 187

By modeling your logic-circuit design in software before, or in place of, building a hardware prototype, you can save yourself a great deal of time and money. Before you can make this determination, however, you must know more about the four basic types of simulation models.—*Kent Moffat and Don Carter, Mentor Graphics Corp*

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VBPA ABP

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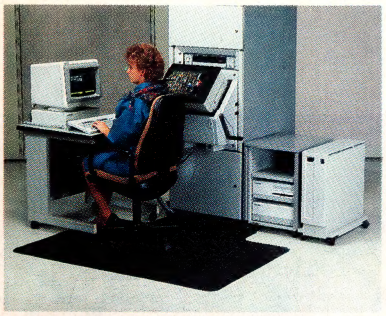
March 17, 1988



***Board- and device-level testability products** are available to proponents of design for testability (pg 57).*

TECHNOLOGY UPDATE

Pioneering engineers begin to adopt board-level automatic test generation 57

KEEPING AMERICA COMPETITIVE

You can recognize a pioneer by the arrow in his back: Despite that adage's implied warning, some designers of board-level products are beginning to adopt design methodologies compatible with testability techniques like automatic test-pattern generation (ATPG). —*Dan Strassberg, Associate Editor*

Customer training and reverse engineering promise to escalate the acceptance of CASE 73

CASE (computer-aided software engineering) is only now reaching the stage of maturity that CAE tools were at several years ago, but it won't be long before CASE catches up to CAE.—*Chris Terry, Associate Editor*

Digitally programmable 1-chip filters yield lower-cost data-acquisition systems 83

Monolithic filters that combine programmability with the proven advantages of switched-capacitor technology promise to let engineers develop less-expensive, more versatile data-acquisition systems.—*Tarlton Fleming, Associate Editor*

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TekCASE™: HOW TO BREAK A PROJECT INTO PIECES. AND PUT IT TOGETHER AGAIN.

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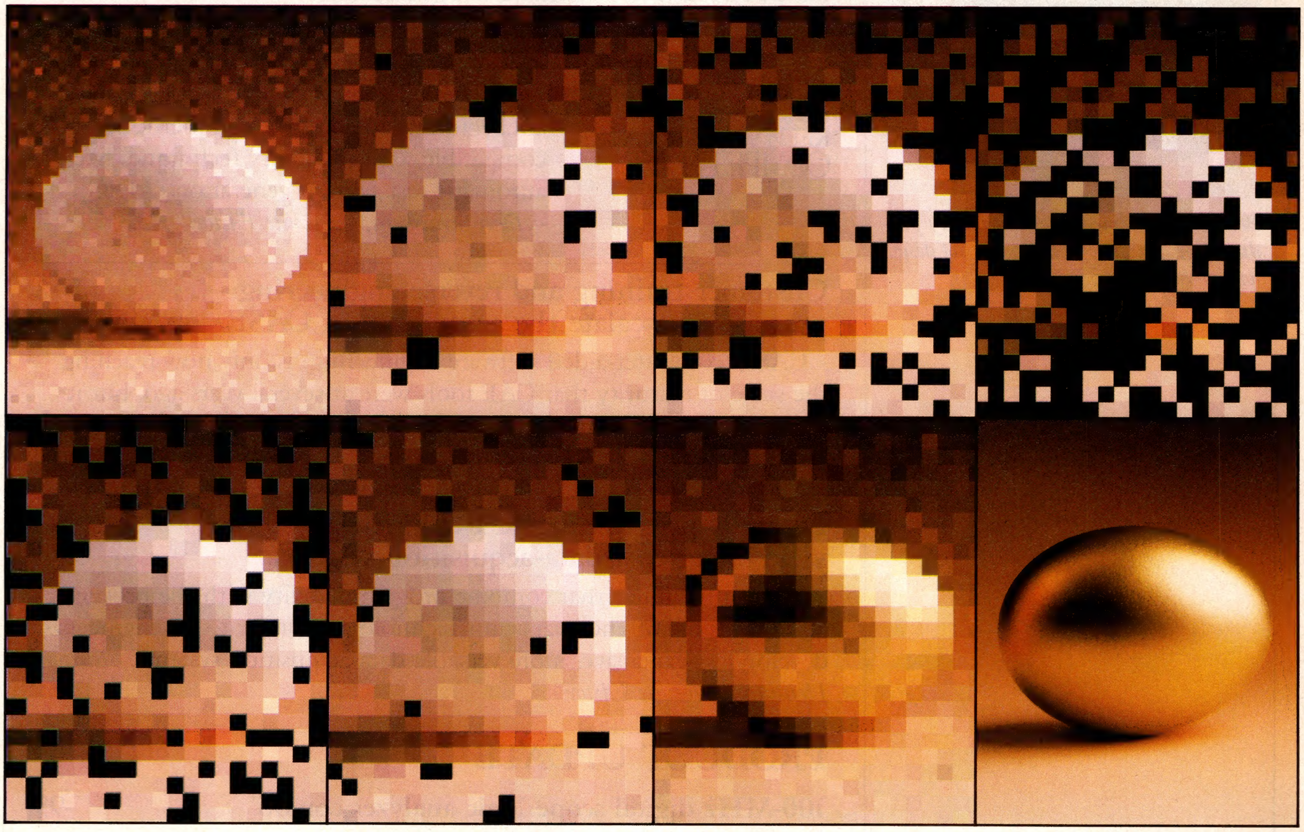

You know how to maintain control and ensure quality of a complex systems project: first you divide it into parts and work on them concurrently, then you put it back together again. You also know how seldom a project survives this kind of reassembly intact—frequently, the final result barely resembles the original intent. Tektronix, a developer of complex systems for many years, now introduces a solution to the problem. This solution is TekCASE: a complete set of software engineering tools and services to guide you through the specification, design, and documentation of even the largest and most complex systems projects. Tektronix supports the entire software development life cycle.

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March 17, 1988

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A magazine like EDN cannot survive for long without a following of loyal, involved readers.

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Ability—not disability—makes the engineer. *Deborah Asbrand, Associate Editor*

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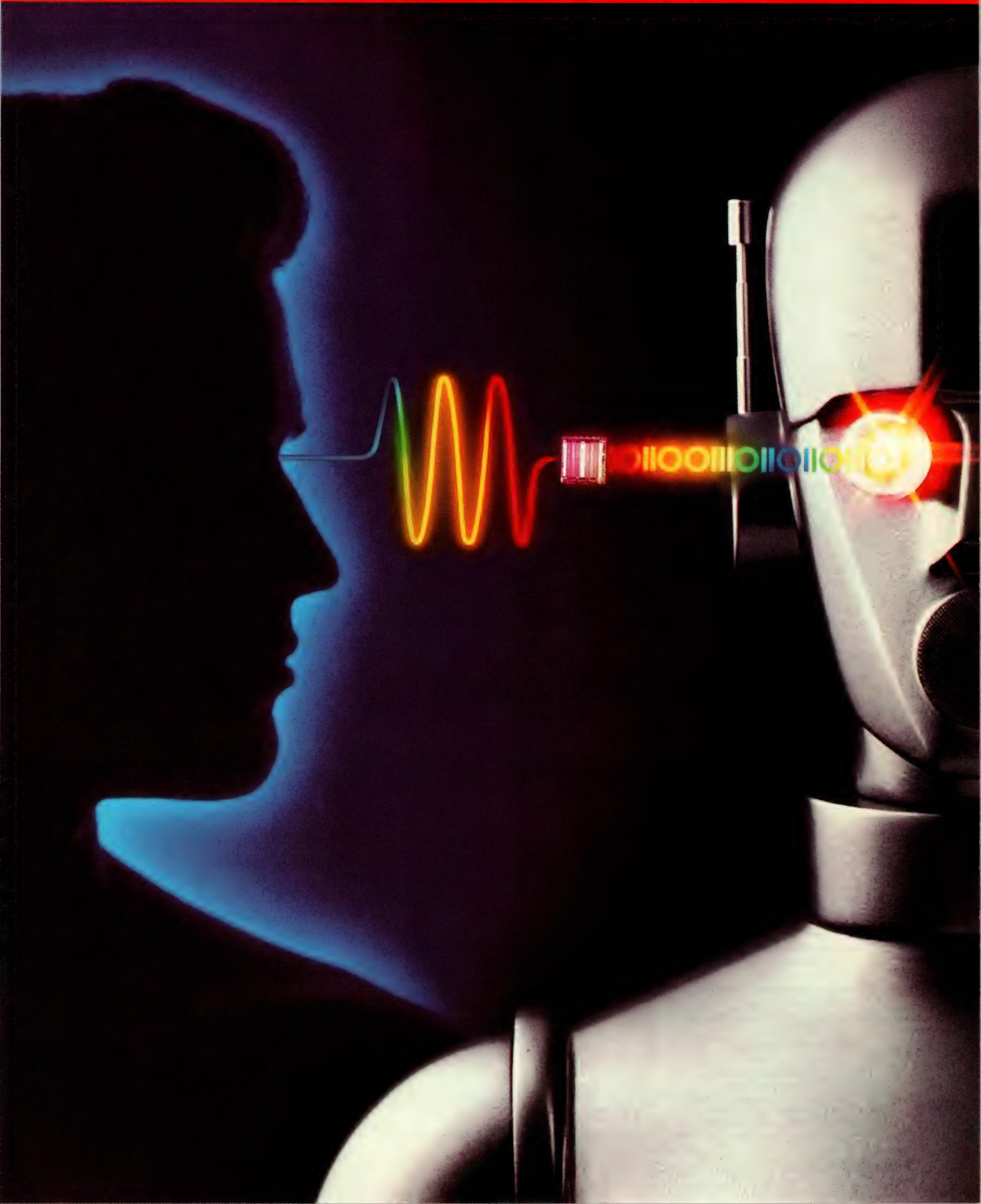
High-resolution conversion



in the blink of an eye.

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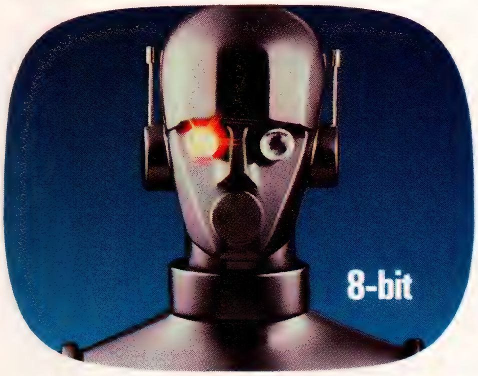

We've expanded our line to include more CMOS flash ADC's, a charge balancing ADC, an SPI ADC and a DAC. All featuring single 5V supply operation.

We also offer a new high-speed op amp especially well-suited to driving ADC's or video cables.

4, 6 and 8-bit CMOS flash ADC's.

Choose from 4, 6 and 8-bit ADC's. All operate at video speeds, with clocking speed and input bandwidth specified at 5V. What makes these flash ADC's special is silicon-on-sapphire construction, resulting in low cost, high speed, very low input capacitance, low power consumption and inherent latch-up resistance.

10-bit CMOS charge balancing ADC.

This 10-bit successive approximation ADC captures fast moving signals, providing excellent resolution.

It features a built-in fast track and hold, with conversion rates of 150 KHz and an input bandwidth of 1.5 MHz. Even at the maximum rate, power consumption is less than 20 mW.

10-bit CMOS serial ADC.

The CDP68HC68A2 is selectable for either 8- or 10-bit resolution and has an 8-channel multiplexer allowing up to 8 channels of inputs. The device can be used directly with our CDP68HC05C4, C8 or D2 microprocessors or other similar SPI (Serial Peripheral Interface) buses.

8-bit CMOS R-2R video-speed DAC's.

These CMOS/SOS digital-to-analog converters operate from a single 5V supply at video speeds and can produce "rail-to-rail" output swings. Typical update rate is 50 MHz. Settling is fast (20 ns typical) to 1/2 LSB. "Glitch" energy is minimized by segmenting and bar graph decoding of upper 3 bits.

High-speed op amp.

Specially designed for use with data converters, the CA3450 op amp has excellent speed and transmission line driving capabilities.

For 10-bit accuracy, it settles to within 1/2 LSB in 40 ns with a 2V input signal. And it can drive up to four 50 ohm transmission lines.

ADC's	*Res. Bits*	*Conv.Rate Hz*	*Power Diss. (MW)*	*Pkg. Leads*	*1K Price*
CA3304E	4	20M	30	16	2.95
CA3304AE	4	25M	35	16	4.50
CA3306CE	6	10M	65	18	5.50
CA3306E/3306AE	6	15M	70	18	6.25/11.25
CA3318E/3318CE	8	15M	150	24	38.50/24.00
CA3310E/3310AE	10	150K	15	24	6.00/8.00
CDP68HC68A2E	10	10K	15	16	3.75
DAC's					
CA3338E/3338AE	8	50M	100	16	6.00/8.40
OP AMP	*UGBW Hz*	*Slew Rate (X10)*	*I_{OUT} MA*	*Pkg Leads*	*1K Price*
CA3450E	200M	300V/μSec	±75	16	2.70

Data in a flash.

For data sheets of these new products, call toll-free 800-443-7364, extension 19. Or contact your local GE Solid State sales office or distributor.

In Europe, call: Brussels, (02) 246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

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Communicate now with our family of protocol controllers.

Our MC68000 Family offers three different protocol controllers to handle all your data communication needs; whether it's across the building or around the world there's a Motorola device that will make your job easier. With our '68000 Family you can choose the protocol and system designs that get you on line quickly and economically.

X.25 Protocol Controller 1984 CCITT X.25 LAPB.

The MC68605 Protocol Controller (XPC) implements the 1984 CCITT Recommendation X.25 Link Access Procedure Balanced (LAPB) for U.S. and European T1 applications. By generating link-level commands and responses, the XPC relieves the host processor of communication link managerial tasks. It's also fully DDN and Telenet certifiable.

Our XPC features an optional transparent mode which allows the implementation of other HDLC-based protocols, with user generation of all frames. The XPC handles full-duplex synchronous serial data rates up to a maximum 10 Megabits Per Second (Mbps) for high-speed computer links.

Multi-link LAPD Controller CCITT Q.920/Q.921 LAPD.

The MC68606 Multi-link LAPD (MLAPD) Protocol Controller fully implements CCITT Recommendation Q.920/Q.921 Link Layer Access Procedure (LAPD) protocol for ISDN networks. The MLAPD is designed to handle both signalling and data links in high-performance ISDN primary rate applications.

This VLSI device provides a cost-effective solution to ISDN link-level processing with simultaneous support for up to 8K logical links. The MC68606 is an intelligent communications protocol controller compatible with AT&T specifications for ISDN devices and features low power consumption and high performance, with an aggregate data rate in excess of 2.048 Mbps.

Token Bus Controller IEEE 802.4 MAC.

The MC68824 Token Bus Controller (TBC) is the only single-chip solution to implement the IEEE 802.4 Media Access Control (MAC), specified by Manufacturing Automation Protocol (MAP). The TBC implements four levels of message priority and the Request With Response (RWR) frame type to meet the real-time needs of factory floor communications and MAP 3.0.

The TBC conforms to the IEEE 802.4G standard MAC to Physical layer serial interface to support broadband, carrierband, and fiber optic networks. The TBC's low power consumption coupled with its extended temperature range versions make it ideally suited for factory automation applications.

Token Bus Frame Analyzer Software speeds development of token bus networks.

The MC68KTBFA Token Bus Frame Analyzer Software (TBFA) is a real-time software tool that speeds development of token bus networks. The TBFA keeps track of statistics while monitoring network performance. By using the simple menu-driven interface, the user can define triggers to selectively store and display frames, creating a powerful tool for network analysis.

The TBFA is a set of four EPROMs which runs on a VMEbus MVME372 Token Bus Controller board and requires a modem, a VT100 terminal, and a power source. The cost-effective TBFA sells for about one-tenth the cost of existing token bus protocol analyzers.

For more information.

For more information about solutions to protocol controller applications contact your Motorola sales office. For technical literature on any of the MC68000 Family of protocol controllers, please complete and submit the coupon below.

We're on your design-in team.

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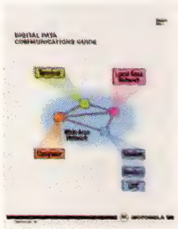

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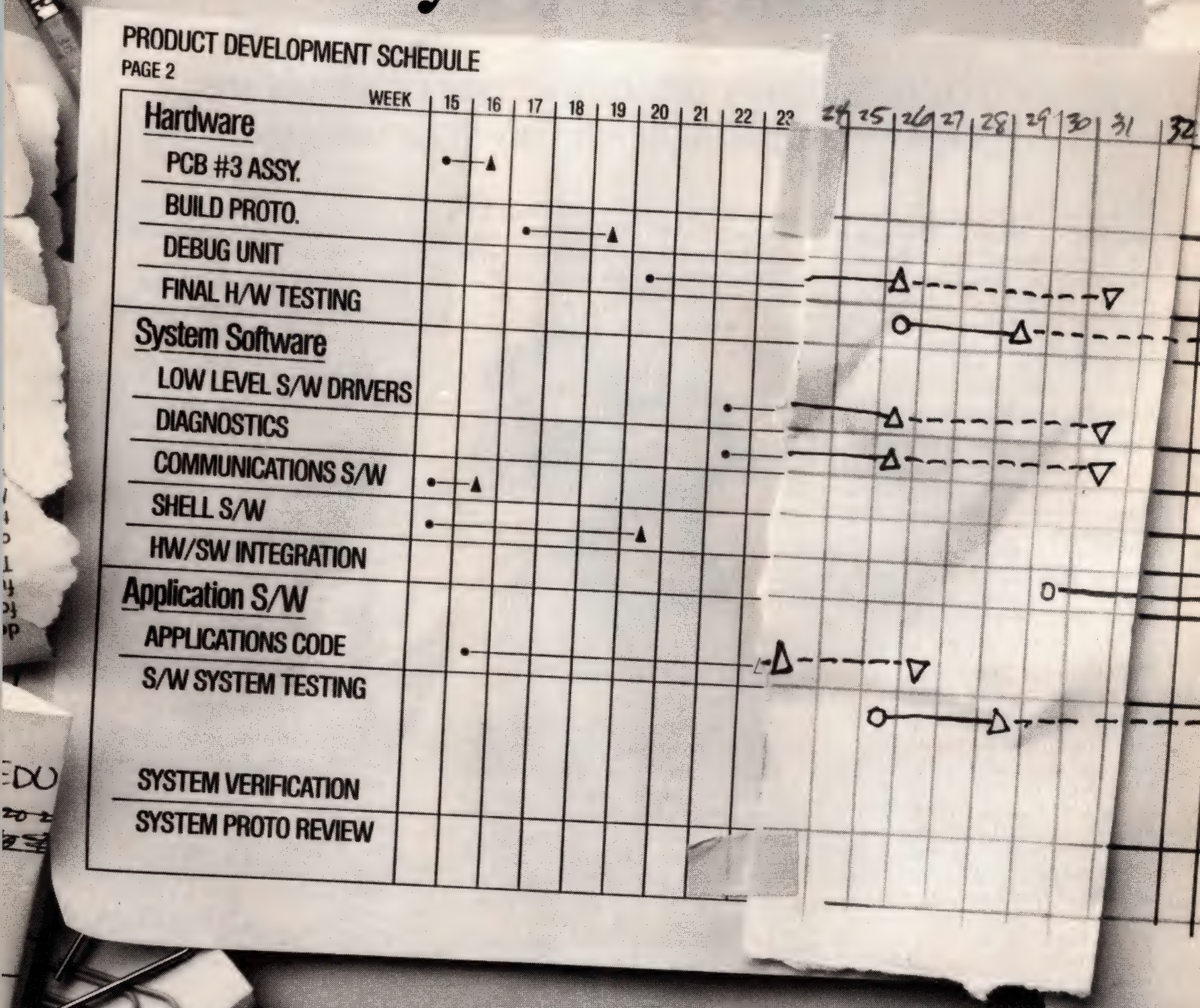


PRODUCT DEVELOPMENT SCHEDULE
PAGE 2

WEEK 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32

Hardware
- PCB #3 ASSY.
- BUILD PROTO.
- DEBUG UNIT
- FINAL H/W TESTING

System Software
- LOW LEVEL S/W DRIVERS
- DIAGNOSTICS
- COMMUNICATIONS S/W
- SHELL S/W
- HW/SW INTEGRATION

Application S/W
- APPLICATIONS CODE
- S/W SYSTEM TESTING
- SYSTEM VERIFICATION
- SYSTEM PROTO REVIEW

Let's face it.

Slipped development schedules and budget overruns can mean lost opportunities. Yet many traps that seriously delay a development schedule are quite complex, especially when they are compounded by problems that arise in cross development work.

Like not knowing whether the errors you are getting from your prototype processor are real. Or losing bugs in the cracks between your development system and the prototype.

Fortunately, the answer to these complex problems is simpler than you might think. Because now Applied Microsystems offers what we call performance packages: complete, fully integrated development solutions, designed to meet your development requirements and to detect even subtle problems quickly.

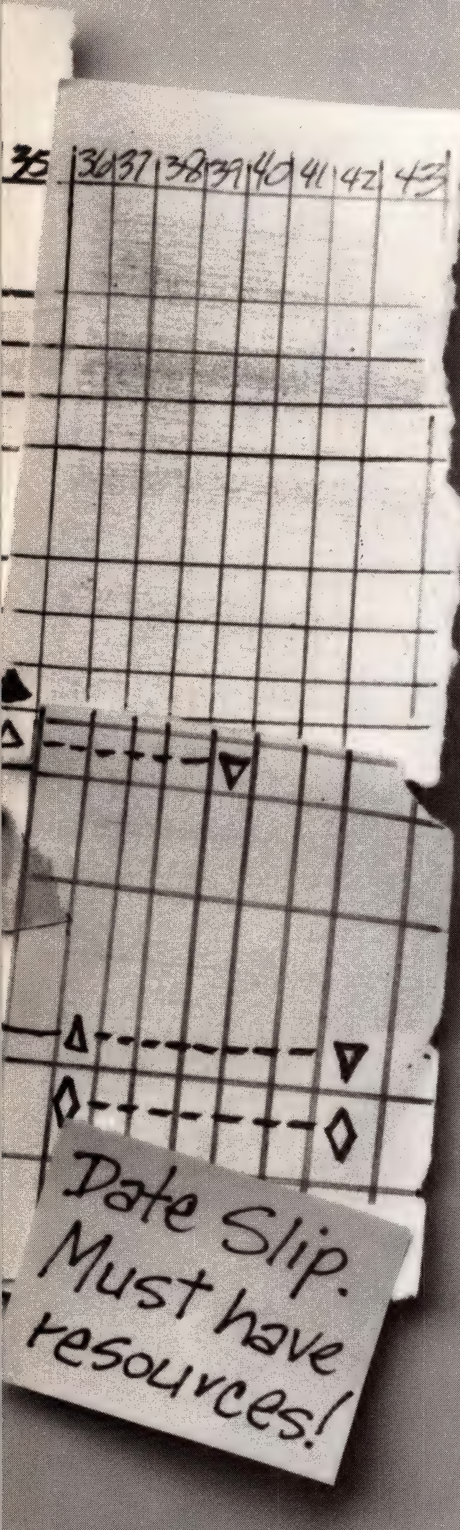
Performance Packages that Live Up to Their Name.

Each package includes a powerful in-circuit emulator, the only tool that can successfully bridge the gap between host computer and prototype. With features like complex triggering, reliable memory, built-in target diagnostics, I/O simulation, and special interrupt handling.

And to complement the power of our emulators, we provide software tools that work with a variety of platforms and languages.

Whichever package you choose, you're getting the highest performance

Invest now or pay later.

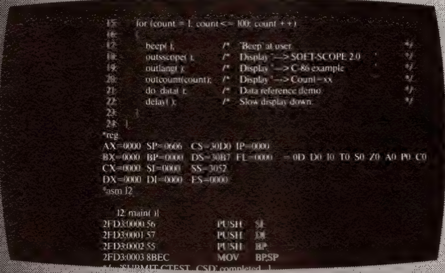


development tools available.

Source Level Debugging for Intel Microprocessors

Our VALIDATE/Soft-Scope and VALIDATE/Soft-Scope 286 packages are designed for any language producing complete Intel OMF information.

A PC-based, in-circuit source level debugger and simulator are closely coupled with our ES 1800 emulator. You can use commands to examine variables on the fly, check contents of registers, and determine current position in code. And real-time trace is displayed as source level statements, machine instructions or bus cycles.



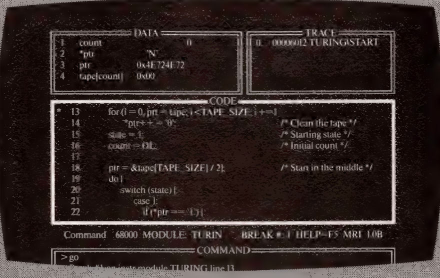
```
15:     for (count = 1, count <= 100: count ++)
16:     {
17:        beep( ):            /*  'Beep' at user.                    */
18:        outsscope( ):       /*  Display '—> SOFT-SCOPE 2.0    '    */
19:        outlang( ):         /*  Display '—> C-86 example      '    */
20:        outcount(count);    /*  Display '—> Count=xx               */
21:        do_data( ):         /*  Data reference demo                */
22:        delay( ):           /*  Slow display down.                 */
23:     }
24: }
*reg
AX=0000  SP=0606   CS=30D0  IP=0000
BX=0000  BP=0000   DS=30B7  FL=0000    = 0D  D0  I0  T0  S0  Z0  A0  P0  C0
CX=0000  SI=0000   SS=3052
DX=0000  DI=0000   ES=0000
*asm 12

    12: main( ){
2FD3:0000 56              PUSH    SI
2FD3:0001 57              PUSH    DI
2FD3:0002 55              PUSH    BP
2FD3:0003 8BEC            MOV     BP,SP
```

The packages also include a logic state analyzer probe, and provide up to 2 Megabytes of overlay memory plus full protect mode support for the 80286.

Source Level Debugging for Motorola Microprocessors

The window-oriented VALIDATE/XEL package combines our XEI source-level debugger, a simulator and the MCC68K compiler with our ES 1800 emulator. The package also includes a logic state analyzer probe and our well-known SCSI interface option, that significantly decreases download time.

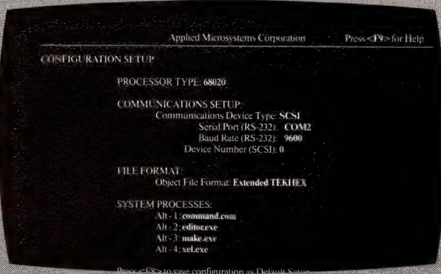


```
=================DATA==================  ============TRACE=============
 1   count                  0             0    0000602 TURING\START
 2   *ptr          'N'
 3   ptr           0x4E724E72
 4   tape[count]   0x00
=================================CODE==================================
*  13      for (i = 0, ptr = tape, i < TAPE_SIZE, i += 1)
   14          *ptr++ = '0';                     /* Clean the tape */
   15      state = 1;                            /* Starting state */
   16      count = 0L;                           /* Initial count */
   17
   18      ptr = &tape[TAPE_SIZE] / 2];          /* Start in the middle */
   19      do {
   20          switch (state) {
   21              case 1:
   22                  if (*ptr == '1') {
 Command   68000  MODULE: TURIN     BREAK # 1  HELP=F5  MRI 1.0B
===============================COMMAND=================================
>go
```

In addition to up to 2 Megabytes of overlay memory, you get target control from your source code; powerful "C" language macros for code patching, remote control and simulation of I/O; plus user-definable windows for viewing registers, stacks and variables

High-speed Symbolic Debugging for Intel, Motorola and Zilog Microprocessors

Our VALIDATE/ES DRIVER package includes easy-to-use (menu-driven and remote control) software that smoothly links the host functions to the ES 1800 emulator. This allows the upload and download of programs, symbol tables and command files.



```
                  Applied Microsystems Corporation          Press <F9> for Help
------------------------------------------------------------------------------
CONFIGURATION SETUP

          PROCESSOR TYPE: 68020

          COMMUNICATIONS SETUP:
                Communications Device Type: SCSI
                       Serial Port (RS-232):  COM2
                       Baud Rate (RS-232):    9600
                    Device Number (SCSI): 0

          FILE FORMAT:
                Object File Format: Extended TEKHEX

          SYSTEM PROCESSES:
                Alt - 1: command.com
                Alt - 2: editor.exe
                Alt - 3: make.exe
                Alt - 4: xel.exe
```

Also included are a logic state analyzer probe; the SCSI option for increasing download speeds by up to 30 times; plus up to 2 Megabytes of overlay memory.

To find out more about 8, 16 or 32-bit development solutions that save money in the long run, write Applied Microsystems Corp., P.O. Box 97002, Redmond, WA 98073-9702. Or call 1-800-426-3925 (In Washington, call 206-882-2000).

In Europe, contact Applied Microsystems Corporation Ltd., Chiltern Court, High Street, Wendover, Aylesbury, Bucks, HP22 6EP, United Kingdom. Call 44-(0)-296-625462.

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CIRCLE NO 11

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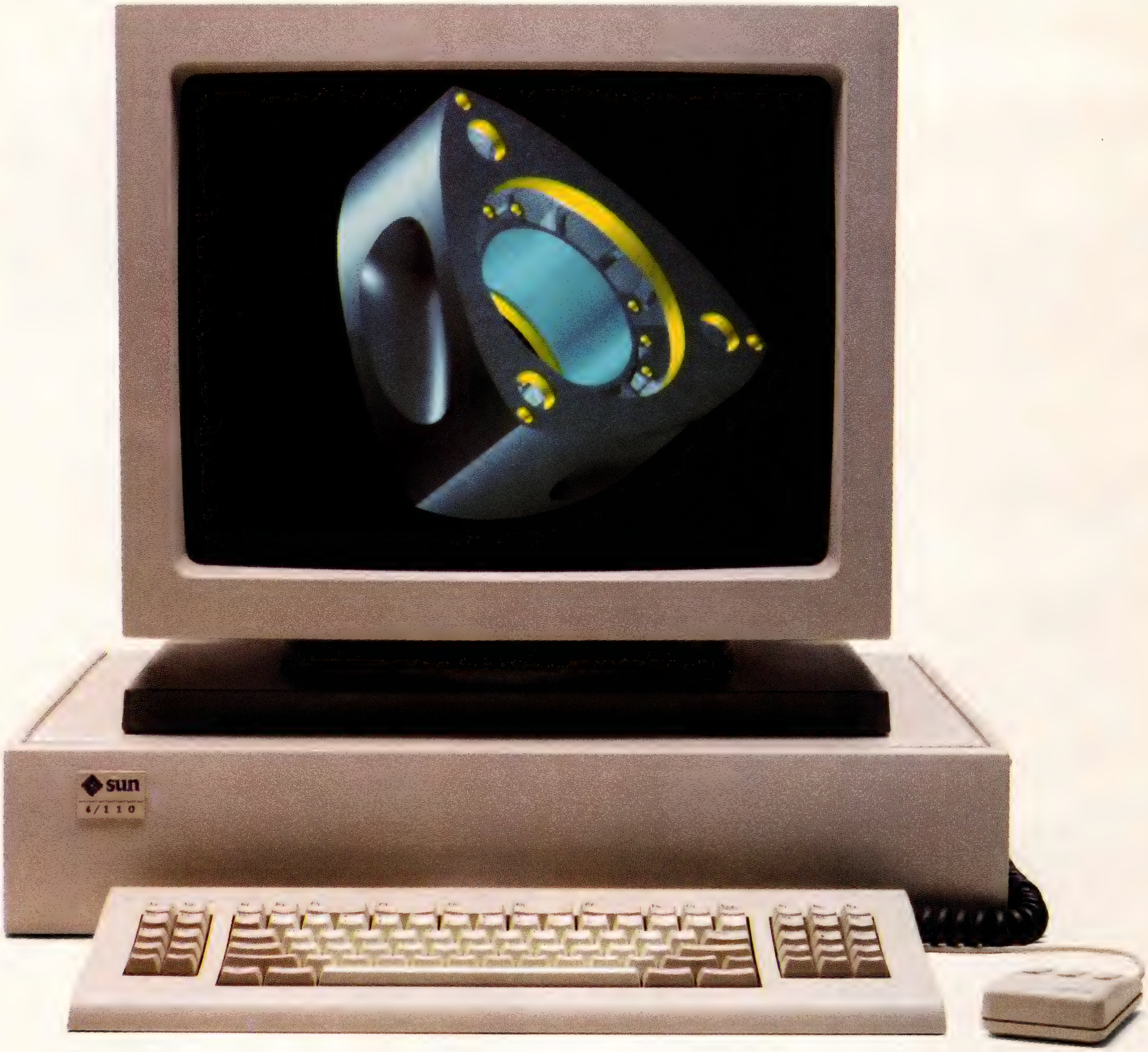

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SUN-4/110. THE FIRST SUPERCOMPUTING DESKTOP WORKSTATION.

This is the newest member of our extensive SPARC™ (for Scalable Processor ARChitecture) family of binary-compatible supercomputing workstations.

Sun-4/110 is a full 32-bit RISC machine that runs at a blistering 7 VAX® MIPS and .8 double precision Linpack MFLOPS.

It also has an ultra-smart, ultra-fast memory management unit that keeps memory active so it—and you—can run at processor speeds.

Its graphics performance is just as thrilling. There's an optional 3-D graphics accelerator you can plug right in, plus a dedicated, pipelined, frame buffer bus that moves solid and wire frame models so fast, you'll think you're at the movies.

You can crunch numbers with the same dispatch thanks to an optional floating-point accelerator.

And you can expand main memory to a very hefty 32 Mbytes.

Which reminds us, the Sun-4/110's main memory has a unique caching scheme. It dynamically allocates up to 32 Kbytes of its static column random access memory to cache. So it's there when you need it. Yet, since it's really just a part of main memory, it doesn't cost you extra.

You see, the object here wasn't just to build a small, fast workstation.

It was to build a balanced workstation that delivers true supercomputing performance from every corner of its being.

That just happens to sit on a desk.

And costs far less than a comparable machine.

So there is no comparable machine.

When is a desktop workstation not a paperweight? When it has this much software support.

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- *Earth Resources*
- *ECAD*
- *Electronic Publishing*
- *Engineering Graphics*
- *Expert Systems*
- *FEA*
- *Financial*
- *Fluid Dynamics*
- *Graphics*
- *Imaging*
- *Layout Verification*
- *Logic/Fault Simulation*
- *Machining*
- *Math & Stat*
- *MCAD*
- *Molecular Modeling*
- *Numerical Control*
- *Schematic Capture*
- *Seismic Processing*
- *Silicon Compilation*
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- *Solids Modeling*
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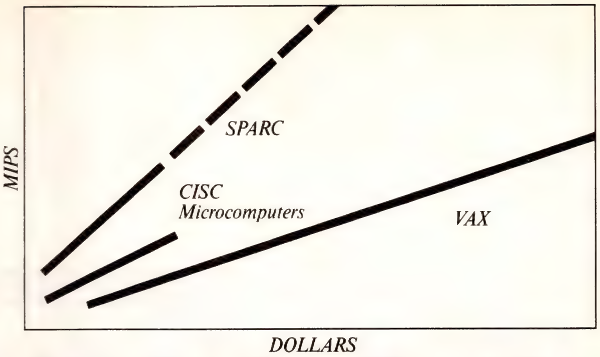
- *Styling & Appearance Modeling*

SIT DOWN IN FRONT OF EVERY COMPUTER IN THE COMPANY.

The great power of Sun-4/110 allows you to now perform compute intensive applications on your own, right at your desk.

But its openness also allows you to run, transparently, any other computer in the company on your own, right at your desk. Thanks to Sun's Open Systems Network (OSN™). The most comprehensive open system offering in the industry.

In addition, Sun-4/110 is designed to run the Sun Operating System (SunOS™), a converged version of UNIX System V and UNIX 4.3/4.2BSD, that has, for the first time, a standard window system (X11/NeWS™), and a standard network file system.



Sun-4's Scalable Processor ARChitecture (SPARC) sends computing in a whole new direction.

Not only is the Sun Operating System compatible with the huge base of existing UNIX applications, it also will conform to the new application binary interface (ABI) standard which will allow you to run any and all SPARC-based applications, straight off-the-shelf.

And because ours is an open, non-proprietary Operating System—specifically designed for high performance computing, by the way—you can be sure there are going to be a lot of its applications around.

Not to mention lots of machines from lots of vendors to run them.

THIS IS WHERE YOU'LL WANT TO BE FROM NOW ON.

Every member of our SPARC-based Sun-4™ family, the Sun-4/110 included, incorporates another high performance standard.

The SPARC chip. An open, non-proprietary 32-bit RISC-based microprocessor.

SPARC chips are being built under license by some of the world's premier semiconductor houses. So they'll be competitively priced.

But unlike every microprocessor that's gone before, SPARC's scalability provides an uninterrupted growth path.

In fact, SPARC has so much headroom, in five years, it'll allow us to deliver a system that runs 100 MIPS.

For the price of a workstation.

SPARC's extendability even includes other Sun workstations. And allows us to upgrade Sun-3/110 and 3/140 systems to Sun-4/110s with a simple board swap.

For more information about the new Sun-4/110 and the SPARC standard, call us at 800-821-4643, or 800-821-4642 in California. Or write Sun Microsystems, Inc., 2550 Garcia Ave., Mountain View, CA 94043.

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CIRCLE NO 12

New high performance PC-based emulators from HP.

Introducing the HP 64700 Series emulators. Low-cost, entry-level, PC-based emulators with features you won't find with any others in the price range—or even higher. The HP 64700s deliver unmatched capability, ease-of-use, measurement power, flexibility, and reliability . . . plus HP support.

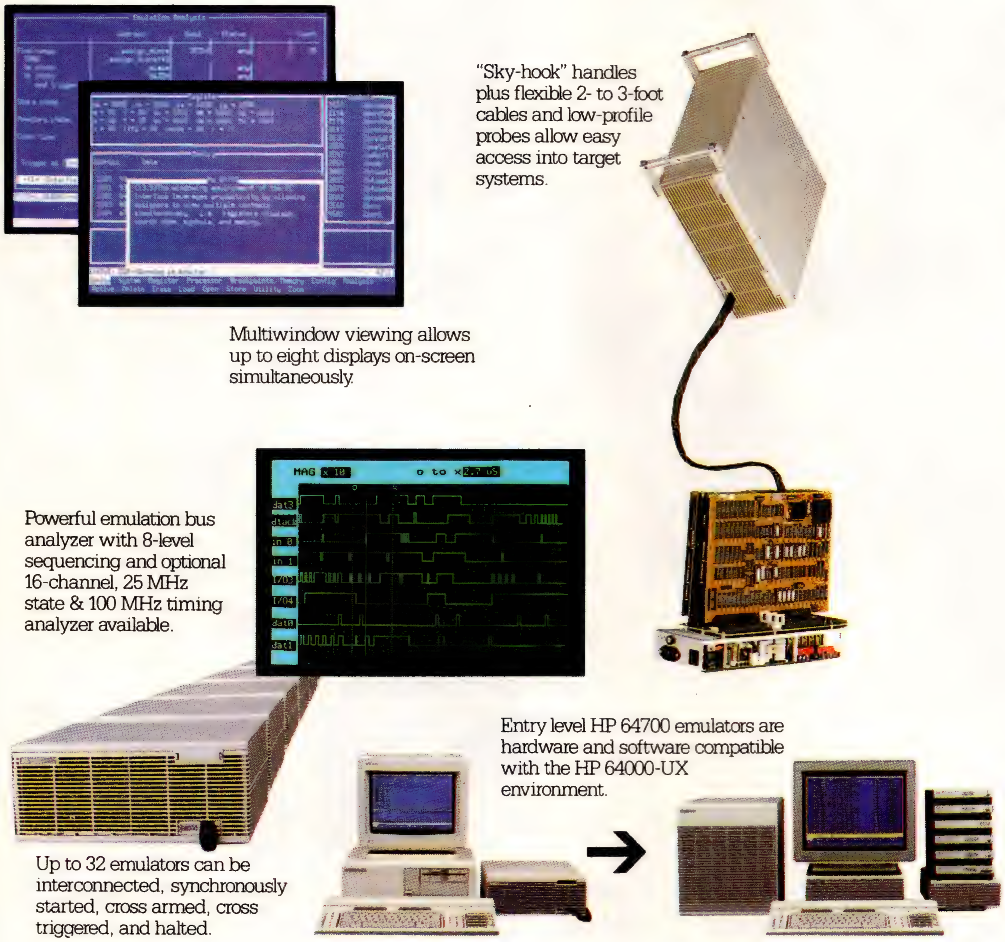
While the HP 64700s are tailored to meet the needs of individual engineers and small design teams, they'll perform equally well for large teams working on complex projects.

The rapidly expanding family of HP 64700 emulators provide real-time, transparent emulation at full processor speeds with no wait states. The PC user interface gives a new meaning to the term "friendly" with features like multiple windows, single-letter keystroke command entry, access to symbols for powerful debugging capability, timing diagrams, and on, and on, and on. The experienced user as well as the beginner will appreciate how easy these emulators are to work with.

In addition to the features shown above, there are lots of others that put the HP 64700s in a class by themselves. To name a few: function with IBM-PC, HP Vectra and compatibles, RS-422 high-speed serial *we never stop asking*

"What if..."

You could spend a lot more and get a lot less.



"Sky-hook" handles plus flexible 2- to 3-foot cables and low-profile probes allow easy access into target systems.

Multiwindow viewing allows up to eight displays on-screen simultaneously.

Powerful emulation bus analyzer with 8-level sequencing and optional 16-channel, 25 MHz state & 100 MHz timing analyzer available.

Entry level HP 64700 emulators are hardware and software compatible with the HP 64000-UX environment.

Up to 32 emulators can be interconnected, synchronously started, cross armed, cross triggered, and halted.

interface for superior download and upload speed, code coverage analysis for efficient software testing and design, host-independent portability, and compatibility with popular absolute file formats such as Tektronix and Intel hexadecimal and Motorola S record.

Once you get your hands on an HP 64700 emulator, you'll agree that this is the new standard in the field. Especially at a starting price of $8,900.

Free demo disc.

For a free demo disc that gives you the "hands-on" feel for HP 64700 Series capabilities, call HP at 1-800-752-0900 ext. 215N, or mail the attached business reply card.

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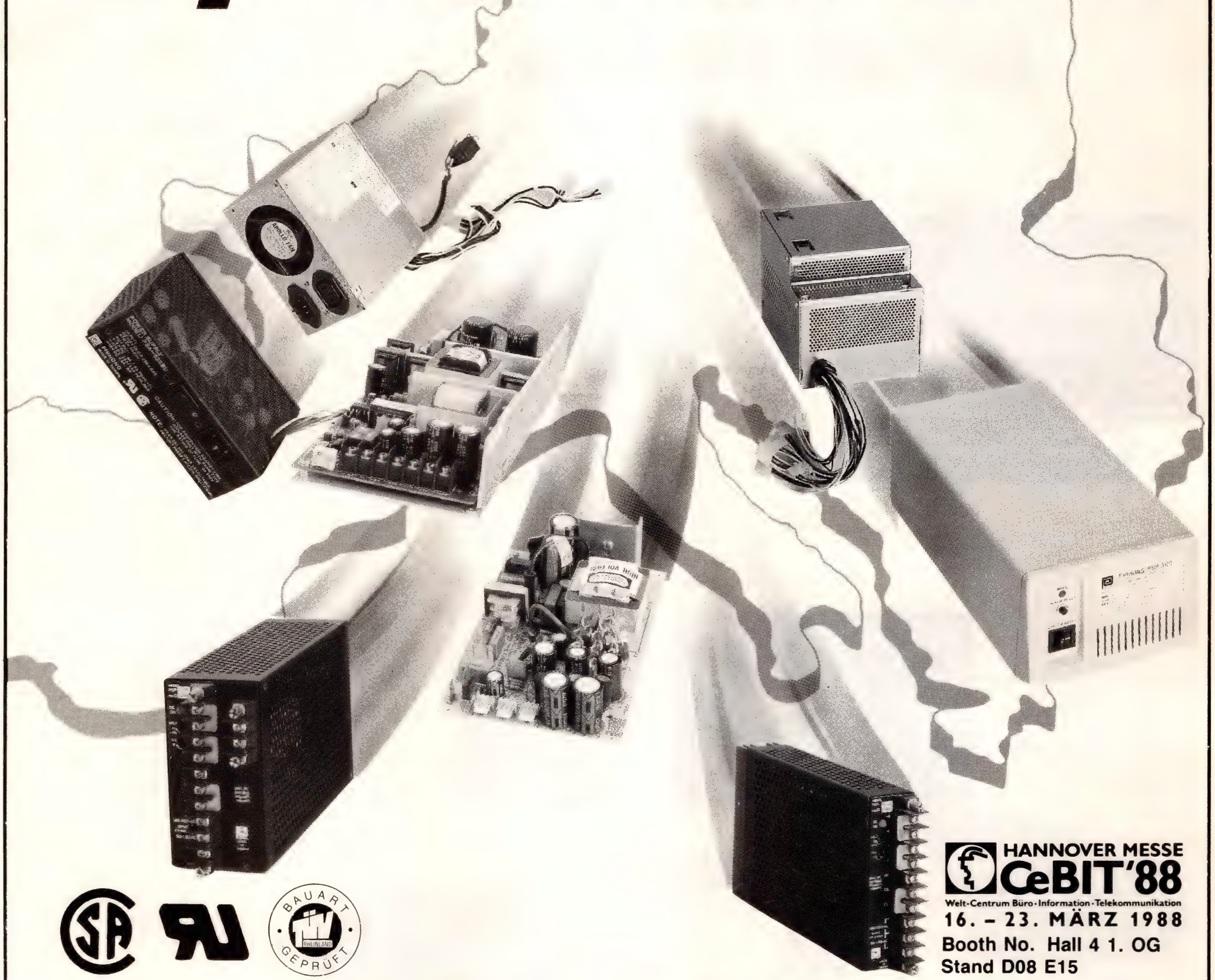

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CIRCLE NO 15

NEWS BREAKS

EDITED BY JOANNE CLAY

BUS-DRIVING, BiCMOS ASIC FEATURES 72-mA OUTPUTS

The LDD10000 family of gate arrays from LSI Logic (Milpitas, CA, (408) 433-8000) lets you create an ASIC that directly drives μP and peripheral I/O buses. Members of the family share a 3-region architecture consisting of I/O modules, internal BiCMOS blocks, and a compacted CMOS core array. The six products that comprise the family contain an estimated 8000 to 45,000 usable CMOS and BiCMOS gates and 144 to 256 I/O pads. You can configure each I/O buffer as an input (with CMOS, TTL, or Schmitt-trigger input characteristics) or an output (with 6-, 12- or 24-mA drive). In addition, you can gang as many as three I/O buffers to create a 72-mA driver. The I/O modules include test circuitry that supports boundary-scan testing. Nonrecurring engineering (NRE) charges for the LDD10000 family range from $100,000 to $250,000, depending on design complexity and factory support. Part costs range from $50 to $500, depending on part complexity and packaging.—Steven H Leibson

ARRAY-PROCESSOR BOARDS ADD COMPUTATIONAL POWER TO PCs

The DSP32-PC family of floating-point array processors from Communications Automation & Control (Bethlehem, PA, (215) 865-9706) are based on AT&T's DSP32 floating-point DSP chip. The products include an 8M-flop processor on an IBM PC half card and a full-size, 25M-flop processor card that's compatible with the IBM PC/AT. Designers who develop computation-intensive applications such as signal processing, graphics, CAE/CAD/CAM, image processing, and scientific applications can employ the processors to run their software on a personal computer. The company also offers software-development tools, including assemblers, user-friendly window-based emulators, C compilers, libraries, and demonstration programs. The IBM PC version of the DSP32-PC is available now; it costs $695 in single quantities. The IBM PC/AT version will cost $1500 and will be available for delivery by the beginning of the fourth quarter of 1988.—Maury Wright

FLOATING-POINT PROCESSOR OFFERS 32-WORD REGISTER FILE

The WTL 3364 floating-point processor from Weitek Corp (Sunnyvale, CA, (408) 738-8400) can execute 20M flops. Integrated on one chip is a 64-bit floating-point multiplier, a 64-bit floating-point ALU, a divide/square-root unit, and a 32-word×64-bit register file with six ports. This chip conforms fully to the IEEE standard for binary floating-point operations. The on-chip register file minimizes bus traffic and allows you to use the multiplier and ALU simultaneously with independent operands. In addition, the divide/square-root unit can operate in parallel with the multiplier and ALU. The 3364 has three 32-bit I/O ports configured as one input port, one output port, and one bidirectional port. You can also use these ports as one 64-bit bidirectional port. The WTL 3164 is functionally identical to the 3364, except that the 3164 has only one 32-bit bidirectional I/O port and comes in a 144-pin PGA (pin-grid array) package. The WTL is mounted in a 168-pin PGA. Samples of both chips are available now; volume deliveries will begin in July. The WTL 3364 costs $909 (10); the WTL 3164 sells for $829 (10).—Doug Conner

UTILITY CONVERTS MS-DOS CODE TO EXECUTABLE 68020 CODE

You can employ the binary-to-binary code-conversion facility provided by XDOS to convert IBM PC-compatible programs for direct execution on Unix-based systems. Hunter Systems (Mountain View, CA, (415) 965-2400) offers XDOS, a Unix utility program, for 68020-based systems. The software includes a binary compiler that performs the code conversion and an environment emulator that emulates the MS-DOS environment. The end user can simultaneously execute multiple converted IBM PC-compatible programs in Unix windows. The program maps the MS-DOS file environment into Unix, so MS-DOS programs can read and write Unix files. The package also includes a Unix utility that reads MS-DOS files. Programs converted with XDOS are not affected by the MS-DOS limit on 32M-byte disk volumes, and therefore can use the full Unix disk capacity. The software is available now for 68020-based systems. OEMs can license the software on a royalty basis. Suggested end-user pricing ranges from $425 to $2000, depending on the number of users a system supports. You can also expect the company to offer XDOS for systems with non-68020 processors, such as Unix systems based on RISCs (reduced-instruction-set computers).—Maury Wright

FLOATING-POINT PROCESSORS SUPPORT IBM-370 FORMAT

The WTL 2364 multiplier and WTL 2365 ALU from Weitek Corp (Sunnyvale, CA, (408) 738-8400) provide an exact implementation of the IBM-370 Basic Floating-Point Facility standard, the vendor claims. The 2-chip set is capable of performing 32M flops for single-precision operations and 16M flops for double-precision operations. The vendor claims these chips are the only double-precision IBM-format VLSI floating-point processors available. Both chips are available in 144-pin PGA packages. Samples are available now; volume deliveries will begin in June. A 60-nsec chip set is priced at $825 (1000); a 75-nsec chip set costs $700 (1000).—Doug Conner

IEEE-488 MACINTOSH INTERFACE TRANSFERS 800k BYTES/SEC

Providing transparent data translation for as many as 14 IEEE-488 instruments and peripherals, the MacSCSI 488 interface from IOtech Inc (Cleveland, OH, (216) 439-4091) plugs into the SCSI (Small Computer Systems Interface) port of your Apple Macintosh+, Macintosh SE, or Macintosh II computer. It facilitates data transfers from as many as 14 devices to the Macintosh+ and Macintosh SE at 600k bytes/sec, and to the Macintosh II at 800k bytes/sec. The modem-size MacSCSI 488 owes its speed advantage to the fact that it uses no interpreted languages during the data-transfer process. The MacSCSI 488 will not interfere with the operation of any hard-disk drives you may connect to your SCSI port.

You can use either high-level, Hewlett-Packard-style commands or low-level bus-transaction commands when writing IEEE-488 programs for the MacSCSI 488. The $795 unit comes with software device drivers that let you program it in many popular languages, such as Microsoft Basic 3.0, Turbo Pascal, Lightspeed C, VIP, and Hypercard. You also get a memory-resident desk-accessory program that lets you acquire and save data from an IEEE-488 instrument while running any application program on your host computer.—J D Mosley

TOKEN-BUS CONTROLLER SPECS 16-MHz DATA-TRANSFER RATE

Besides boosting the speed of its Enhanced TBC token-bus controller, Motorola (Austin, TX, (512) 440-2140) has cut the price by 43% and packaged the controller in a plastic leaded chip carrier (PLCC). The Enhanced TBC provides a maximum communication speed of 16 MHz. Further, it performs IEEE 802.2 Logical Link Control Type 3 acknowledged connectionless services, which increase the controller's performance and decrease the volume of the program code you have to write. The controller can operate at serial data rates as low as 10 kHz. You can use the Enhanced TBC for local PBX backplane connections, or you can use it to avoid protocol conversion in field buses, providing a simple and inexpensive MAP interface. Available in 10-, 12.5-, and 16-MHz versions, the Enhanced TBC starts at $43.30 (100).—J D Mosley

TRW LSI
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genuine TDC1048
performance in
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CIRCLE NO 16

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NEWS BREAKS: INTERNATIONAL

NETWORK SUITS REAL-TIME CONTROL AND DATA ACQUISITION

The Efiway industrial-control network from Efisystème (Montluel, France, TLX 340821) allows you to control as many as 8064 distributed I/O lines from a Multibus I computer or an IBM PC/AT. The token-ring network, which employs an optical-fiber cable operating at a bit rate of 3.5M bps, can accommodate as many as 63 computers or I/O stations. Communication between a computer and the network takes place via dual-port RAM on the computer's network-interface card. The network's automatic-packet-transmission facility transfers the contents of this dual-port RAM to remote I/O locations or into the dual-port RAM of other network computers. It also transfers the input status of remote I/O channels back into the computer's dual-port RAM. These transfers occur automatically, without any software support from the control computer. As a result, the entire system appears to the computer to be a memory-mapped system rather than a network. The company estimates the cost of a 5-station network with one intelligent station at around Fr fr 150,000.—Peter Harold

PROGRAMMABLE AUDIO PREAMP ELIMINATES GAIN-SWITCHING NOISE

By employing multiple-input, switchable op amps, the TEA6300 audio-frequency preamplifier provides electronic volume, bass, treble, and balance controls; an input-source selector; and a quad fader, none of which generate audible noise when you adjust them. Available from Philips' Components Div (Eindhoven, The Netherlands, TLX 51573) for approximately gld 8.50 (10,000), the device is suitable for use in a variety of consumer hi-fi audio equipment. The preamplifier has an overall gain of 20 dB, and it typically introduces 0.05% total harmonic distortion. It has an input sensitivity of 50 mV for full output voltage, a signal-to-noise ratio of 80 dB, and a channel separation of 70 dB typ.

The device's pinout allows you to introduce additional signal-conditioning circuitry between the input source selector and the preamplifier's input. An I^2C-bus interface allows you to program the preamplifier's control settings from a microcontroller. The TEA6300 is supplied in a 28-pin DIP or a surface-mount minipack.—Peter Harold

ANGLO-AMERICAN ACCORD PUTS VRTX32 AND UNIX ONTO VME BUS

Plessey Microsystems Ltd (Towcester, UK, TLX 31628; in the US, Pearl River, NY, (914) 735-4661) and Ready Systems (Palo Alto, CA, (415) 326-2950) have cooperated to produce Vxcel, a software package that supports Ready Systems' VRTX32 real-time operating system on Plessey's 32-bit VME Bus CPU cards. The package not only allows you to use Unix V.3 as a program-development environment, but also lets you integrate Unix and ROM-resident VRTX32 executives in a target system.

Links between the two operating systems allow you to request Unix services from programs running under the VRTX32 executive. The links also let you request real-time services provided under VRTX32 from an application program running in the Unix environment. With Vxcel, you can also use Plessey CPU cards as target systems for software generated by Ready Systems' Cardtools computer-aided software-engineering (CASE) packages, or as targets for Ada programs that use ARTX as their run-time operating system. The companies haven't yet decided on licensing arrangements for Vxcel, but they expect to have the first release of the product ready in the second quarter of 1988.—Peter Harold

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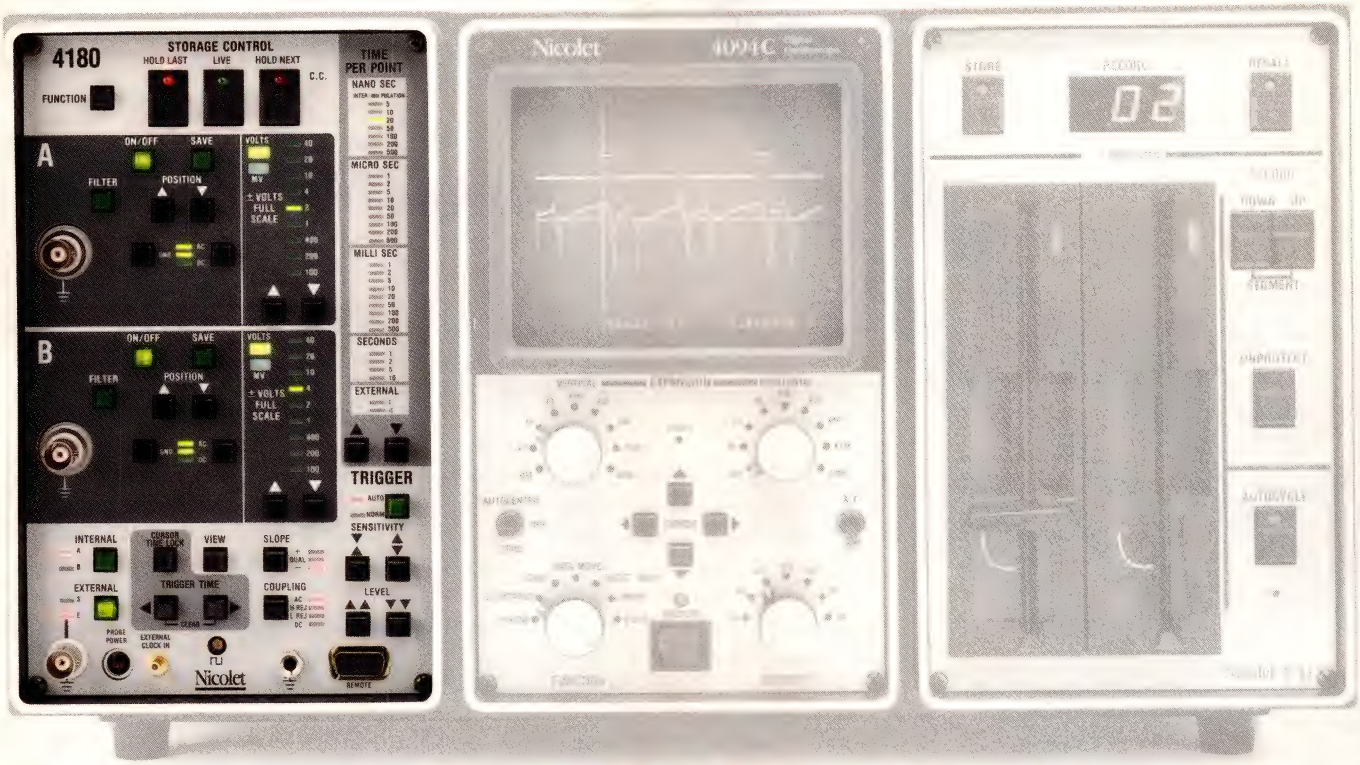

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Real-Time Math. In addition to the extensive post-processing capabilities in the mainframe, the 4180 has several useful routines which present computed results as live, real-time displays: *FFT, MAX/MIN, A+B, A−B, A×B, A/B,* and *AVERAGING.*

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INSTRUMENTS OF DISCOVERY

CIRCLE NO 17

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absorptive... reflective

dc to 4.6GHz from $\$32^{95}_{(1\text{-}24)}$

Tough enough to pass stringent MIL-STD-202 tests, useable from dc to 6GHz and smaller than most RF switches, Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

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Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3n sec switching speed.

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SPECIFICATIONS

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CONNECTOR MODEL	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	−5V on, OV off		−5V on, OV off	
OPER/STOR TEMP.	−55° to +125°C		−55° to +125°C	
PRICE (1-24)	**$32.95** **$72.95**		**$48.95** **$88.95**	

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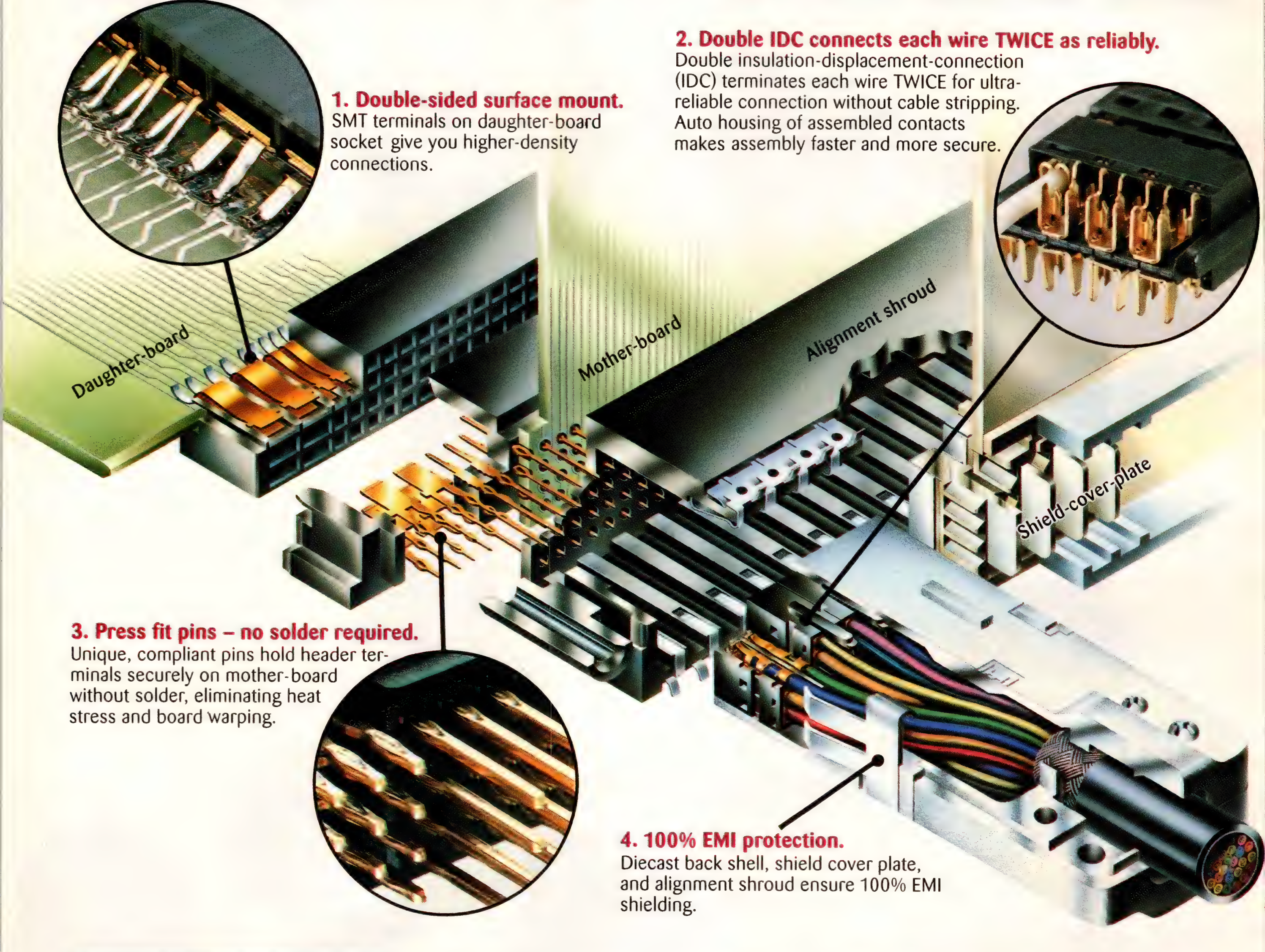
C71 Rev. A

CIRCLE NO 19

"Give me one good reason to change to Fujitsu's FCN-9505/9506 Series connectors."

"One reason? I'll give you FOUR."

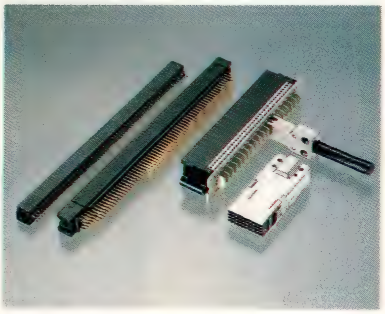


1. Double-sided surface mount.
SMT terminals on daughter-board socket give you higher-density connections.

2. Double IDC connects each wire TWICE as reliably.
Double insulation-displacement-connection (IDC) terminates each wire TWICE for ultra-reliable connection without cable stripping. Auto housing of assembled contacts makes assembly faster and more secure.

3. Press fit pins – no solder required.
Unique, compliant pins hold header terminals securely on mother-board without solder, eliminating heat stress and board warping.

4. 100% EMI protection.
Diecast back shell, shield cover plate, and alignment shroud ensure 100% EMI shielding.



Why buy connectors when you can buy the System, Fujitsu's FCN-9505/9506 connector system? For about the same price as ordinary connectors that fit most of the time, you can buy a complete connector system – SMT sockets, press fit headers, shielded I/O connectors and alignment shrouds – that fits every time.

Higher I/O density

Plus, the System saves space. End-to-end stackable preloaded 8-pin units fit into shielded I/O sockets, and interface directly to mother-board pins, so you can pack I/O connections tighter than ever before.

So, before you place your next connector order, ask your Fujitsu components dealer about the FCN-9505/9506 Series connector system. Chances are he'll give you at least four good reasons to change to the System. And every one means better connections for you.

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CIRCLE NO 20

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Short turn-off delays, high turn-off amplification and low turn-off losses – demands made of GTO technology for modern drive engineering and met by: gate-turn-off thyristors in conjunction with special low-inductance capacitors for power electronics.

In the latest electric locomotives, underground railways and tramcars, machine tools, elevator controllers, UPS installations for computer centers and hospitals: here and elsewhere these low-inductance capacitors have already proven their worth.

The task:
secure limiting of the dynamic load on GTO thyristors in their turn-off phase by reliably handling the voltage spikes with a protective RCD circuit.

The solution:
the GTO capacitor from Siemens.

This application-oriented solution in MKV technology – a recognized quality feature – with its coaxially wound design combines:

- low self-inductance
- high pulse handling capability
- self-healing
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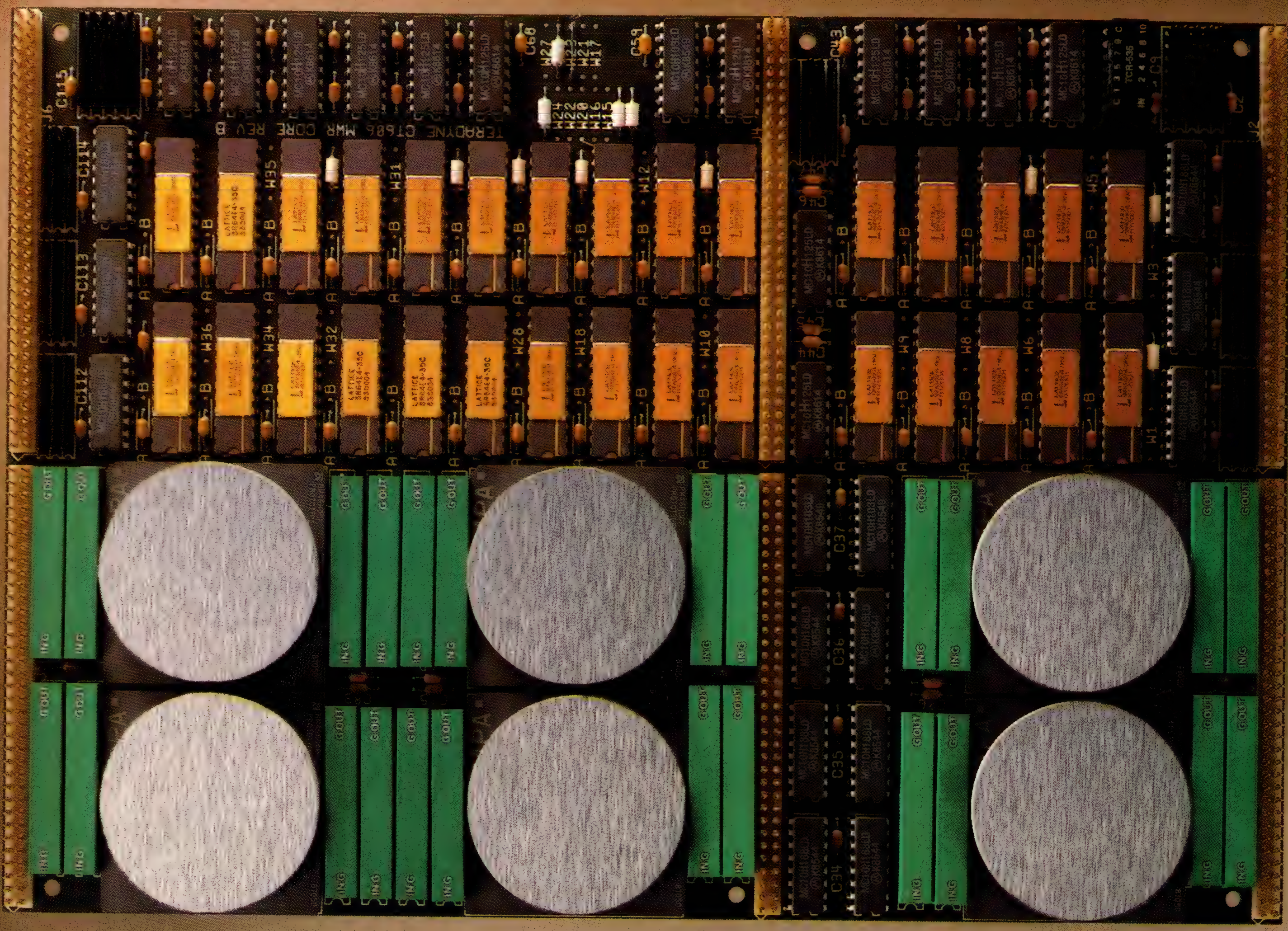
Capacitors
for power electronics
from Siemens

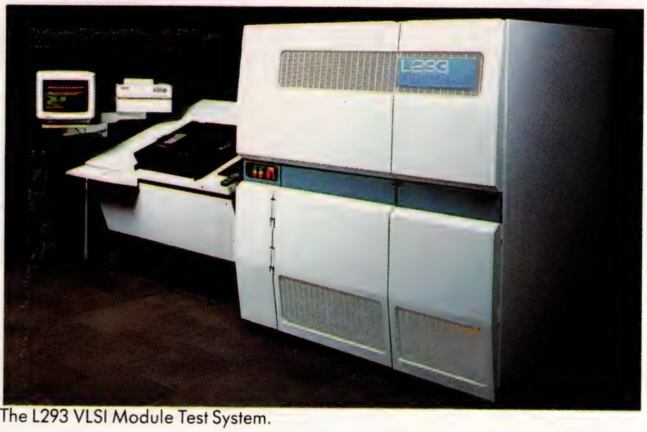
CIRCLE NO 21

12/Z048e



If you're testing complex boards

You're facing one of test engineering's toughest challenges. VLSI boards like this one. But with a Teradyne L200 board tester on your side, complex test problems can be conquered quickly.



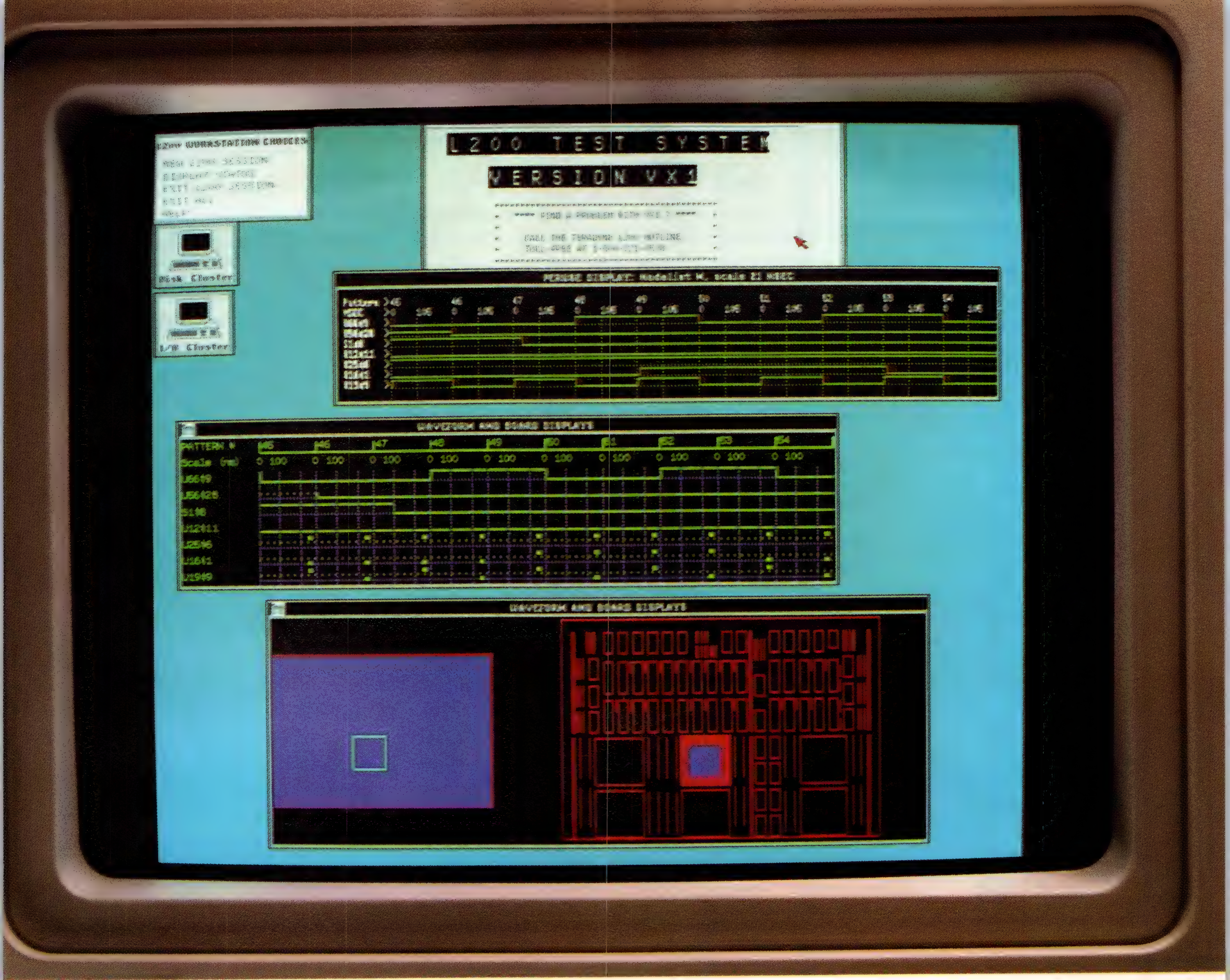
The L293 VLSI Module Test System.

Stay in front of VLSI/VHSIC advances.
Start with the most advanced hardware for analog and digital testing. An L200 fires functional test patterns at 40 MHz rates. At up to 1152 test channels. Top speed is 80 MHz. That's 4 to 8 times faster than any competitor can deliver.

And the L200 hits test signal timing precisely. With up to 32 timing sets for drive phases and test windows. Its 250 ps programming resolution with zero dead time puts signal edges right where you want them.

Divide and conquer.
VLSI/VHSIC boards demand large, complex test programs. But the L200's distributed computer architecture simplifies matters.

Testing is controlled by a VAX computer. It sends tasks to specialized processors for rapid deployment of analog, digital, and memory tests.



here's a simple plan of attack.

Programmers will appreciate clustered VAX workstations. Graphics, like waveforms and shmoo plots, make heavy debug and analysis light work.

Simulation and other tactics.

High-powered software tools tailor L200 test development to modern design techniques and test strategies. Precisely the caliber of tools you need to get tests up and running fast.

	Test Channels	Maximum Pattern Rate	Channel Skew
L297	1152	80 MHz	± 1.5 ns
L293	576	80 MHz	± 1.5 ns
L280vx	1152	10 MHz	± 10 ns
L210vx	576	10 MHz	± 10 ns

L200 VLSI board test systems are the performance leaders.

Take our LASAR simulator. It works closely with the L200 for both cluster and board-level testing. LASAR accurately predicts VLSI circuit responses and reports test program fault coverage.

Significantly, LASAR simulates L200 characteristics. So test programs automatically include when to test board responses. And what response is expected. The result is uncompromising go/no go tests as well as precise guided probe or fault dictionary diagnosis.

A powerful ally.

L200's have proven themselves under fire at hundreds of advanced manufacturing sites worldwide. So if you're about to take on a new VLSI/VHSIC project, find out how to launch a winning test strategy. Call your local Teradyne sales office or write:

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C
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  - PDP-11: UNIX/TNIX/VENIX
  - 68000: UNIX System V
  - PC,XT,AT: MS-DOS
  - PowerNode: UTX/32

UNIX: TM of AT&T Bell Labs.
VAX, VMS, PDP-11, ULTRIX: TM of Dig. Equip. Corp.
TNIX: TM of Tektronix Inc.
VENIX: TM of VenturCom
PowerNode; UTX/32: TM of Gould Inc.

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CIRCLE NO 23

SIGNALS & NOISE

Lost technology?

Recently, two Design Ideas submissions, one written by me and the other by my son, were rejected, showing your reviewers' lack of understanding of the concepts illustrated.

I'd like to solicit your readers' comments on this subject.

In my view, the parameter of transconductance (g_m) characterizes active devices better—whether bipolar transistor, FET, or vacuum tube—than the much more commonly used parameters of current gain or voltage gain (β or μ).

Bipolar and FET devices, as well as electron tubes, are transconductance-controlled devices. Their transconductances are functions of (q/kT) and the device output current (I_O). The reason that standard tube testers and transconductance-type testers give essentially equivalent results is that both respond in the same manner to the deviation from ideal g_m (I_Oq/kT). This deviation increases with I_O, thanks to the increasing cathode (interface) impedance.

At low currents and with minimal leakage, the transconductances of both FETs and electron tubes are (q/kT) times the output currents for the devices. Because edge-current effects increasingly shield the control of channel current as I_O increases, the effective transconductance decreases.

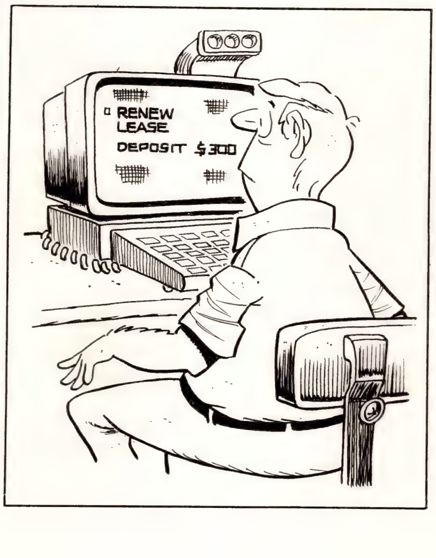
The parameters of importance to all of these devices include the bias voltage used to set a given level of output current and the bias-voltage change necessary to alter the output current by a given ratio (like 2:1). As long as beta exceeds a nominal value like 20, it's unimportant. But both driving point and transfer admittances are functions of the respective currents and define the admittances in terms of (q/kT) and an efficiency parameter. All of these devices have inherently exponential nonlinearities, and the discrepancies are consequences of inherent parasitic parameters like base, emitter, and source spreading resistances and cathode interface impedance. Consequently, the use of current or voltage gain in characterizing these devices leads to analytical errors.

Proper operation of solid-state amplifiers depends on the control of voltage gain. Freedom from oscillation and achievement of minimum-phase characteristics, so vital in color TV and Doppler measuring systems, for example, can only be achieved with amplifiers whose voltage gain is stabilized. And transconductance defines voltage gain.

IEEE publications accept only analytical studies. Publications like EDN can fill the gap between pure theory and applications. EDN needs to encourage articles and Design Ideas that fulfill this goal.

I ask your readers to send in their opinions on this sbject.

Keats Pullen
Kingsville, MD



WRITE IN

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CIRCLE NO 24

NEW FROM TEK: ANALOG FUNCTION, ARBITRARY WAVEFORM AND SWEEP GENERATION IN ONE COMPACT PACKAGE.

The Tek AFG 5101 Programmable Arbitrary/Function Generator is the latest addition to Tek's TM 5000 family of proven, programmable, modular test instruments.

An analog function generator, the AFG 5101 can generate standard sine, square and triangle waveforms, plus dc level, with frequencies from .012 Hz to 12 MHz and amplitudes of 10 mV to 9.99V peak-to-peak, into 50 ohms. Waveforms can be continuous, triggered, gated or burst, from a full range of triggering modes.

With synthesizer option, the AFG 5101 achieves frequency accuracies to .005% (120 Hz to 12 MHz) over and above the .2% frequency accuracies in the standard instrument.

An arbitrary waveform generator, the AFG 5101 uses two independent 12-bit by 8K waveform memories to build any imaginable signal from an array of 8,192 horizontal addresses and 4,096 vertical addresses. Enter the waveforms manually from the front panel, from computer data —or select one of the unit's predefined, 1,000-point waveforms.

A sweep generator, the AFG 5101 includes linear,

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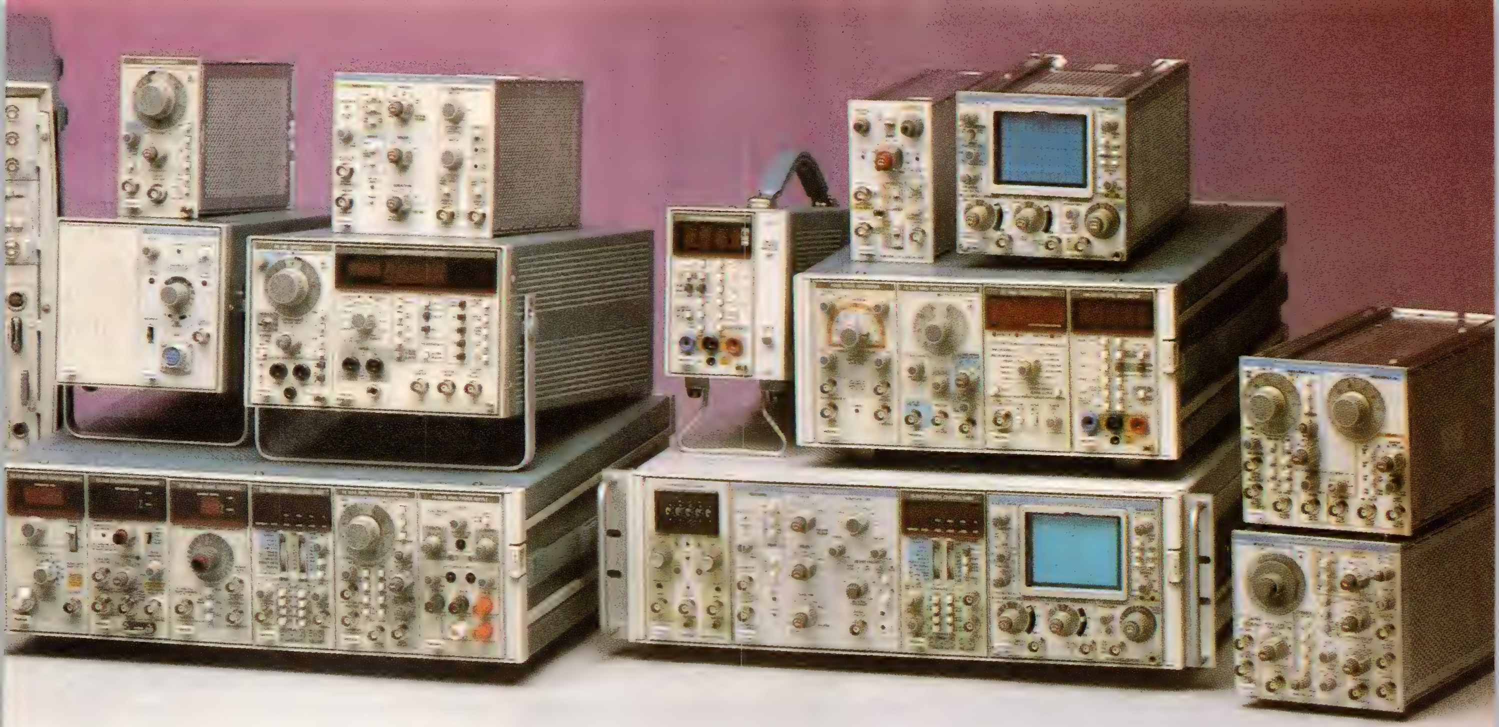

logarithmic and arbitrary sweeps, with any sweep usable in continuous, triggered, gated or burst mode. Users can receive instant frequency readout of breakpoints, notches, or response anomalies.

The applications are wide open. Use the AFG 5101 to drive sensors, timers, and other R&D equipment. To simulate metal stress or vibration characteristics. To teach waveform theory to students. And much more.

Easy waveform editing capabilities ...non-volatile storage of up to 99 front panel settings and two 8K point waveforms...binary block GPIB transfer...two waveform memories plus third, execution memory—these and other features make the AFG 5101 a simple, powerful and uniquely flexible tool.

AVAILABLE IN THREE CONFIGURATIONS.
The first triple-duty test instrument of its kind, it is available in monolithic (AFG 5501), as a plug-in (AFG 5101), or in our Programmable Arbitrary Stimulus/Measurement package (EBS 5002).

Take 10% off with our package offer. Order the AFG 5101 in our Programmable Arbitrary Stimulus/ Measurement package and take 10% off catalog prices.

For the full story on these and other Tek modular instruments, call 1-800-426-2200. Or contact your nearby Tektronix field office.

(Center photo) The AFG 5101 can be ordered in either monolithic version, top right, or as a plug-in for the TM 5000 series mainframes, top left. Or, combine it with the DM 5010 4.5 Digit Multimeter and DC 5009 135 MHz Digital Counter within a TM 5006 mainframe (EBS 5002), as shown at bottom, and take 10% off the normal catalog price.

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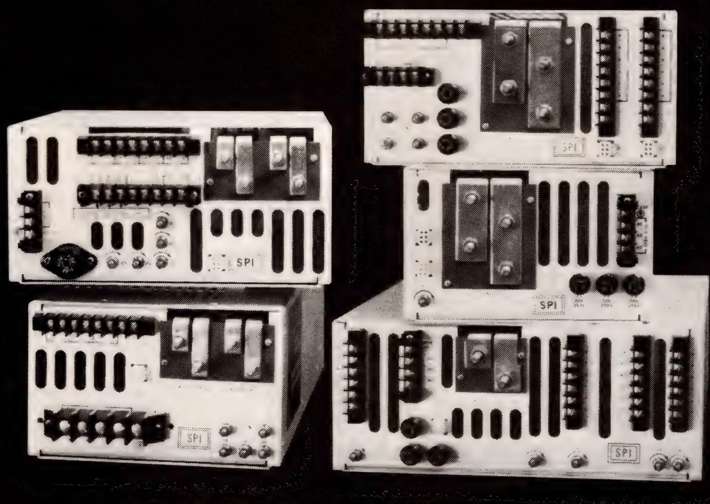
CIRCLE NO 25

So, it's Power you want?



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CIRCLE NO 26

CALENDAR

Visualization Science in Engineering and Computing, Arlington, VA. American College of Radiology, Box 2348, Merrifield, VA 22116. (703) 648-8961. March 30 to April 1.

Digital Signal Microprocessor and Microcomputer Chips and Development Systems (seminar), Cambridge, MA. Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. April 4 to 6.

Worst-Case Circuit Analysis (seminar), Orlando, FL. Design and Evaluation, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043. (609) 770-0800. April 4 to 6.

Microcircuit Interconnections and Assembly Methods (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 7.

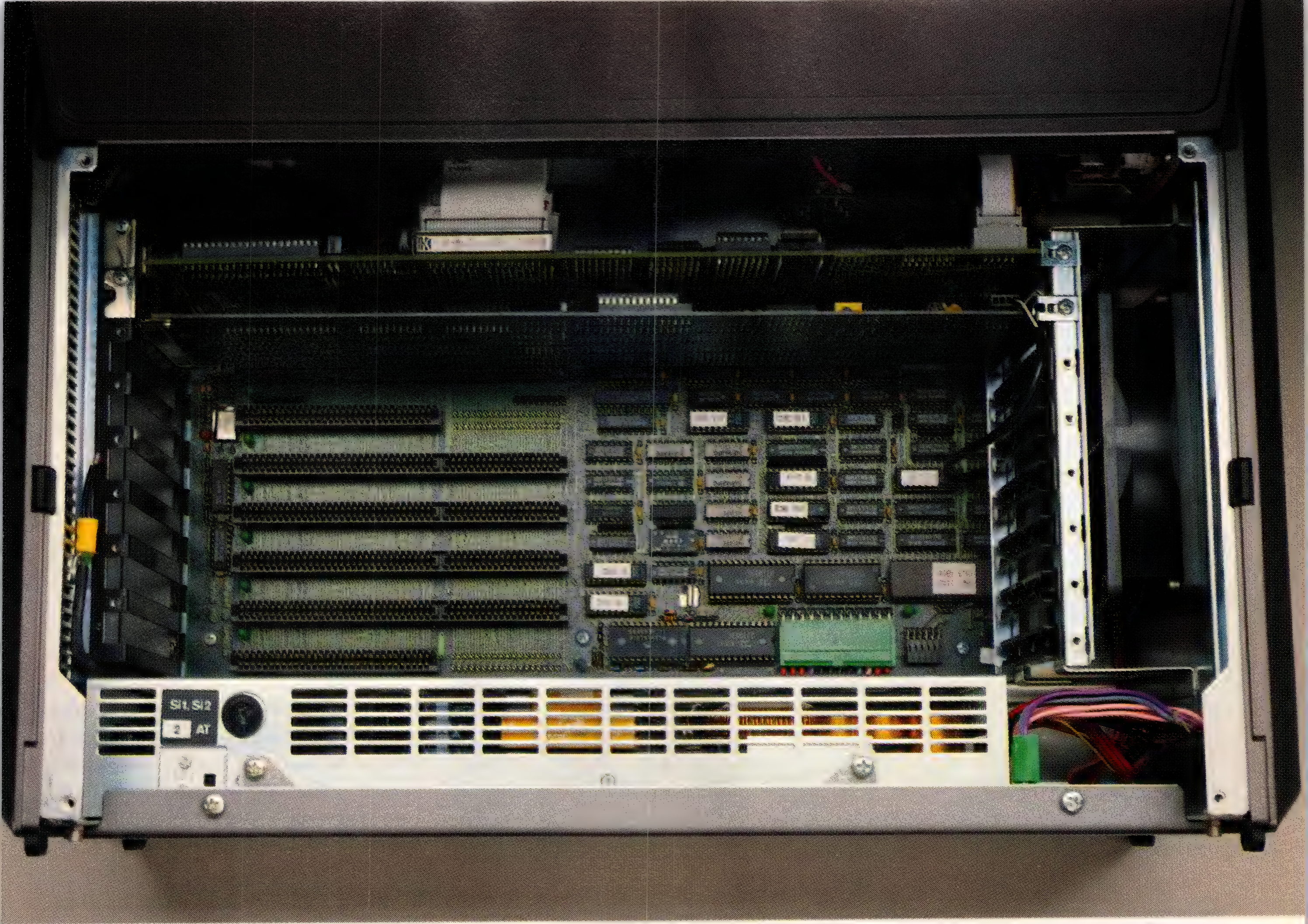
Electrostatic Discharge (ESD): Concern or Over-Concern? (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 12.

Hybrid Microcircuit Technology (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 18.

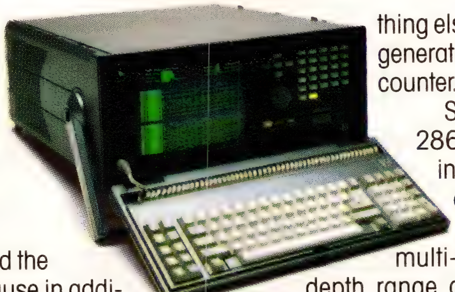
American Power Conference, Chicago, IL. Robert Porter, Illinois Institute of Technology, Chicago, IL 60618. (312) 567-3202. April 18 to 20.

Worst-Case Circuit Analysis (seminar), San Diego, CA. Design and Evaluation, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043. (609) 770-0800. April 18 to 20.

4th International Integrated Services Digital Networks Exposition, St Louis, MO. Information Gate-



We Suggest You Approach Your Logic Analyzer Decision Backwards.



Up front, the PLA 286 gives you more of what you need to solve even the toughest timing problems. Much deeper memory, for example, than you'll find anywhere else: Up to 4K per channel for state analysis; up to 8K for timing. And from 48 up to 112 channels. So you get a much bigger window into problem areas.

But what you see when you look behind the machine may impress you even more. Because in addition to being a powerful logic analyzer, it's also a powerful 10-MHz, 0-wait-state, AT-compatible computer.

There they are. Count 'em.

Six standard slots, waiting to turn the PLA 286 into anything else you want it to be. Now, or later. Pattern generator. Oscilloscope. SCSI tester. Frequency counter. Ethernet node. Whatever.

So when you look at it backwards, the PLA 286 is a very forward-thinking machine, indeed. Fold up the keyboard, grab the handle, and it moves from heavy-duty, complex R&D lab applications, to complete, multi-function field analysis. All the power, depth, range, and flexibility you need for the most demanding software and hardware analysis, in one, neat box.

The PLA 286 is one decision you can back into, and feel great about. Give us a call. (800) 227-8834.

KONTRON ELECTRONICS

United States KONTRON ELECTRONICS INC., 630 Clyde Avenue, Mountain View, CA 94039-7230, Toll free number 800-227-8834
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CIRCLE NO 28

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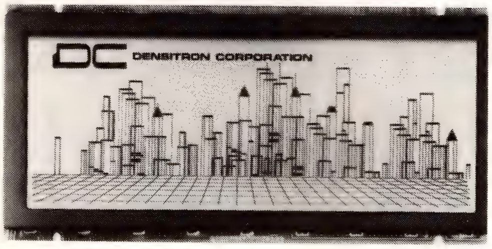

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CIRCLE NO 29

keepers, 214 Harvard Ave, Boston, MA 02134. (800) 323-1088; in MA, (617) 232-3111. April 18 to 21.

Instrument Society of America/IEEE Columbus Conference and Exhibit, Columbus, OH. Sol Black, AT&T Network Systems, Dept 11CB123430, 6200 E Broad St, Columbus, OH 43213. (614) 860-5605. April 19 to 20.

Fiber Optic Communication Systems (short course), Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. April 19 to 22.

IEEE Instrumentation/Measurement Technology Conference (IMtc/88), San Diego, CA. Bob Myers, IMtc, 1700 Westwood Blvd, Los Angeles, CA 90024. (213) 475-4571. April 19 to 22.

Modern Electronic Packaging (seminar), Raleigh, NC. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. April 20 to 22.

Modern Microwave Techniques (short course), Los Angeles, CA. UCLA Extension, 10995 Le Conte Ave, Los Angeles, CA 90024. (213) 825-3344. April 25 to 28.

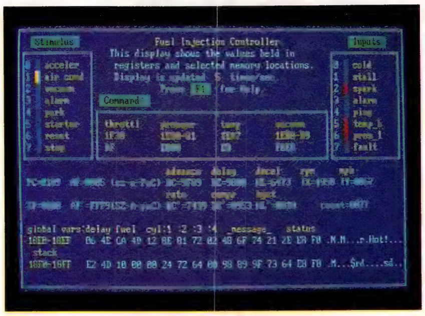
Systems Engineering for Engineers and Managers, Los Angeles, CA. N B Reilly & Associates, 4220 S Harbor Blvd, Suite 305, Oxnard, CA 93030. (805) 985-7413. April 26 to 28.

Uninterruptible Power Systems: Design, Selection, and Specification (short course), Milwaukee, WI. Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N 6th St, Milwaukee, WI 53203. (414) 227-3120. April 28 to 29.

Introducing UniLab 8620 analyzer-emulator with InSight.

- There's nothing like InSight.™ A feature of the new 8620 that lets you actually **watch** your program go through its paces. So you can debug faster. And speed up microprocessor development. For demanding applications like the automotive controller shown.

- An exciting industry first, InSight blends analyzer/emulator techniques to give you continuous, real time monitoring of key processor functions. See changing register contents, I/O lines, ports, user-defined memory windows. With your own labels. And all at once. Interactively. Without stopping your program.



- InSight is made possible by the 8620's advanced bus state analyzer, its 2730-bus-cycle trace buffer, and a new high-speed parallel interface that eliminates RS-232 bottlenecks.

- The fast interface also speeds data throughput. From your hard drive, you can load a 64K program into emulation memory in five seconds.

- On top of that, you get a new, crystal-controlled 1 μsec clock for super precise event timing.

- Computer integrated instruments from Orion prove debugging needn't be costly or tedious. For more than 150 processors. Like all our analyzer-emulators, the 8620 debugs by symptom. Via advanced truth table triggering. Always included is enough breakpointing and single stepping (now faster than ever) to assure optimum efficiency. We even provide a stimulus generator and built-in EPROM programmer to help finish the job.

- Get serious about price/performance. Save big on design, test, and support costs. UniLab 8620 analyzer-emulator.

- Look into it.

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CIRCLE NO 30

VME VIEWPOINT #1

“We don’t plan to let VME rest on its laurels.”

Shlomo Pri-Tal Manager, VME System Architecture and Technology

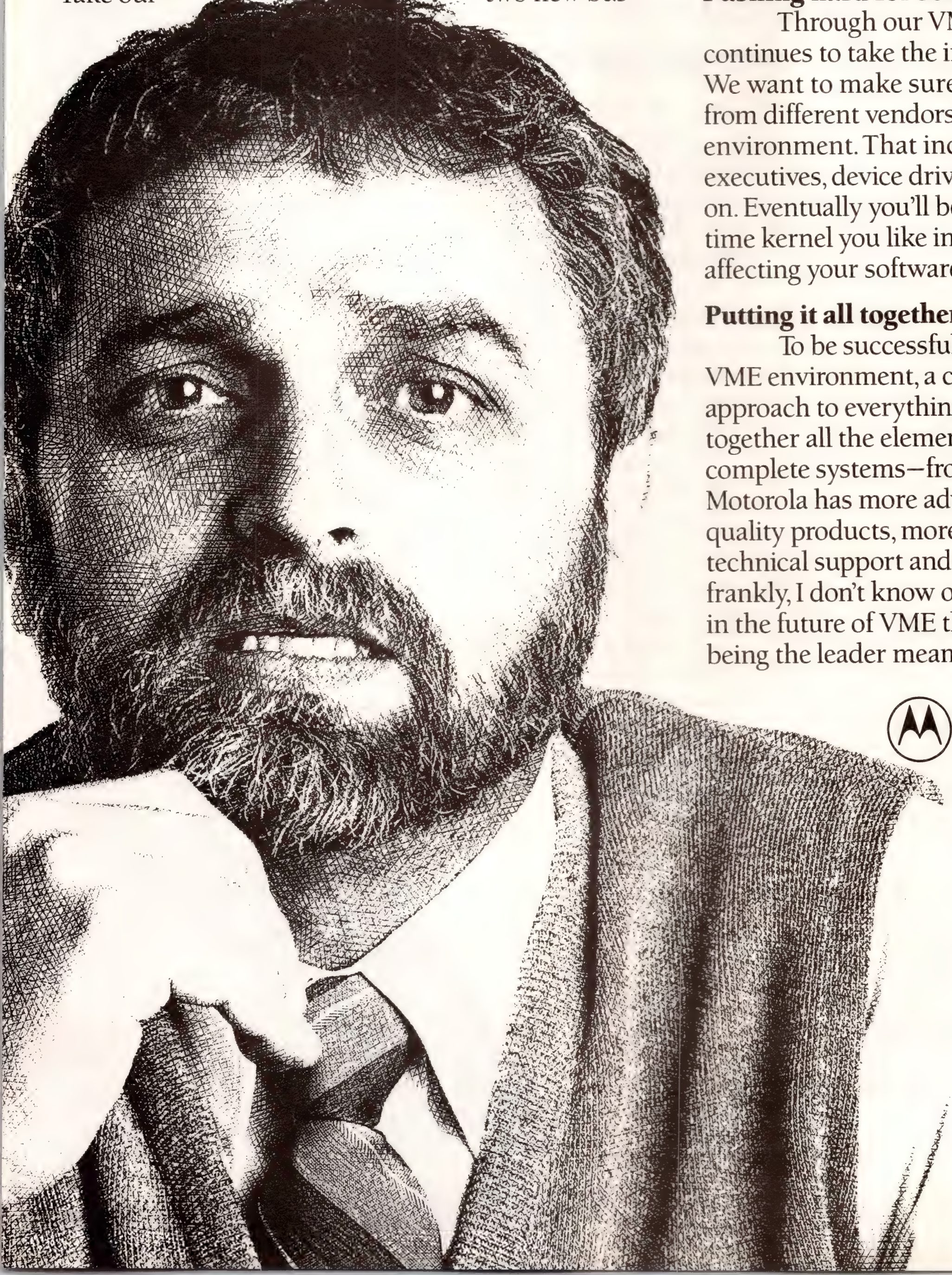
People think Motorola invented VME. Actually, a lot of companies had a hand in developing it. That's one of its main strengths: it's an *open architecture,* with no patents or copyrights to worry about.

Building open systems, to open markets.

In the long run, open systems benefit everyone. That's why we've always fought so hard for VME standardization through VITA, IEEE and IEC. Because standards create a very competitive market, where the OEM has literally thousands of VME choices—from Motorola and elsewhere.

Chipping away at interface standards.

These same standards have enabled Motorola to push bus hardware to higher levels of integration. Take our two new bus interface products, for example—the VME and VSB chips. They eliminate a major source of potential design errors for OEMs. So they can focus on *applications,* rather than bus interface problems.



Plugging in mainframe performance.

To maximize OEM product life cycles, you need a way to keep on plugging in new technologies, without obsoleting your current products. That's exactly what our 68000 family—within a VME architecture—does for you. Right now we have 020-based boards that are more powerful than the mainframes of 10 years ago. And 030 products that put the power of *today's* minicomputers on a desktop.

Pushing hard for software standards.

Through our VMEexec project, Motorola continues to take the initiative in standardization. We want to make sure VME software modules from different vendors work together in a common environment. That includes UNIX,® real-time executives, device drivers, network services, and so on. Eventually you'll be able to plug, say, any real-time kernel you like into a VME board—without affecting your software investment.

Putting it all together.

To be successful in today's more complex VME environment, a company has to take a systems approach to everything it does. That means putting together all the elements—chips, boards, software, complete systems—from a single reliable source. Motorola has more advanced technology, more high quality products, more software resources, more technical support and more VME experience. And frankly, I don't know of anyone who's investing more in the future of VME than Motorola. That's what being the leader means.

MOTOROLA
Microcomputer Division

Approaching our technology from your point of view.

CIRCLE NO 31

For reprints of this series,
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in California, 1-800-441-2345, Ext. 230.
Or write: Motorola Microcomputer Division,
2900 South Diablo Way, Tempe, AZ 85282.
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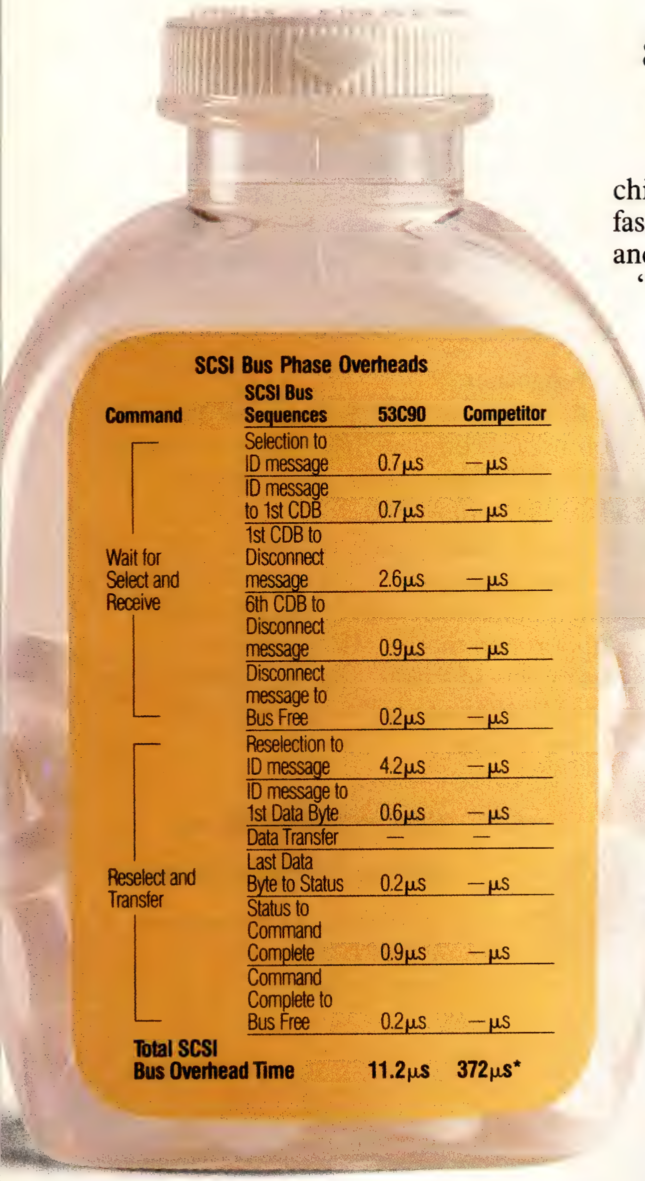
NCR keeps standards

Finally, a cure for SCSI overheadaches.

NCR's 53C90 is the only chip that can give you fast, fast, fast relief from overheadaches . . . and that includes the newest "A" and "6250" versions from the competition.

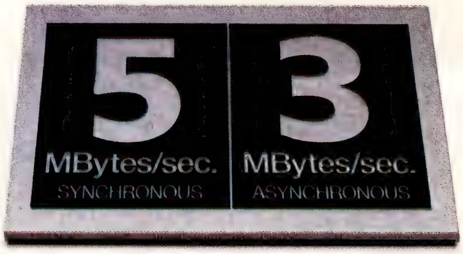
Using combination commands, dedicated sequential logic and dual-ranked registers for command pipelining, the 53C90 is magnitudes faster on and off the bus. Plus NCR implements complex bus sequencing in hardware, not time-wasting software.

Here's our benchmarks. But run your own and you'll see the other guys cause overheadaches, we cure them.



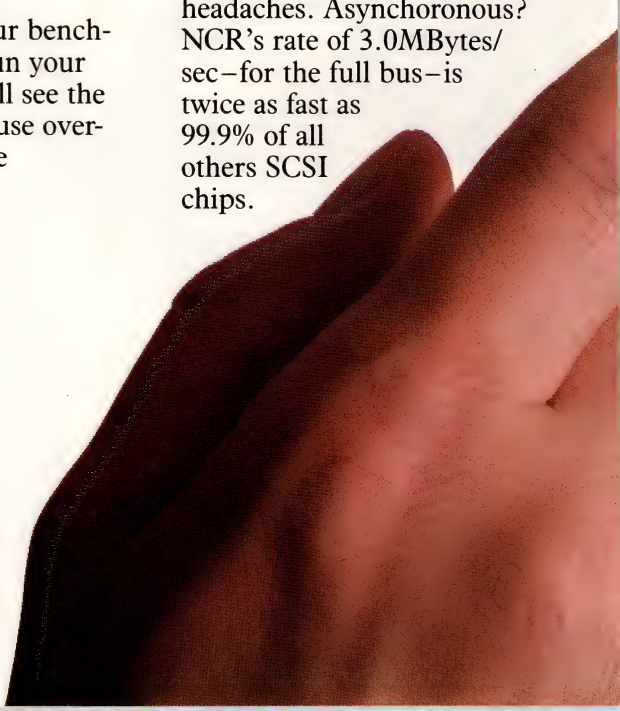
SCSI Bus Phase Overheads

Command	SCSI Bus Sequences	53C90	Competitor
Wait for Select and Receive	Selection to ID message	0.7µs	—µs
	ID message to 1st CDB	0.7µs	—µs
	1st CDB to Disconnect message	2.6µs	—µs
	6th CDB to Disconnect message	0.9µs	—µs
	Disconnect message to Bus Free	0.2µs	—µs
Reselect and Transfer	Reselection to ID message	4.2µs	—µs
	ID message to 1st Data Byte	0.6µs	—µs
	Data Transfer	—	—
	Last Data Byte to Status	0.2µs	—µs
	Status to Command Complete	0.9µs	—µs
	Command Complete to Bus Free	0.2µs	—µs
Total SCSI Bus Overhead Time		**11.2µs**	**372µs***



How our data transfer rates rate.

You either got great numbers. Or you don't. We got 'em. NCR 53C90 delivers the SCSI bus maximum of 5.0 MBytes/sec synchronous at 25 MHz for the full length of the bus. That's at least 1MByte/sec better than most competitive chips can do, without migraine-sized overheadaches. Asynchoronous? NCR's rate of 3.0MBytes/sec–for the full bus–is twice as fast as 99.9% of all others SCSI chips.



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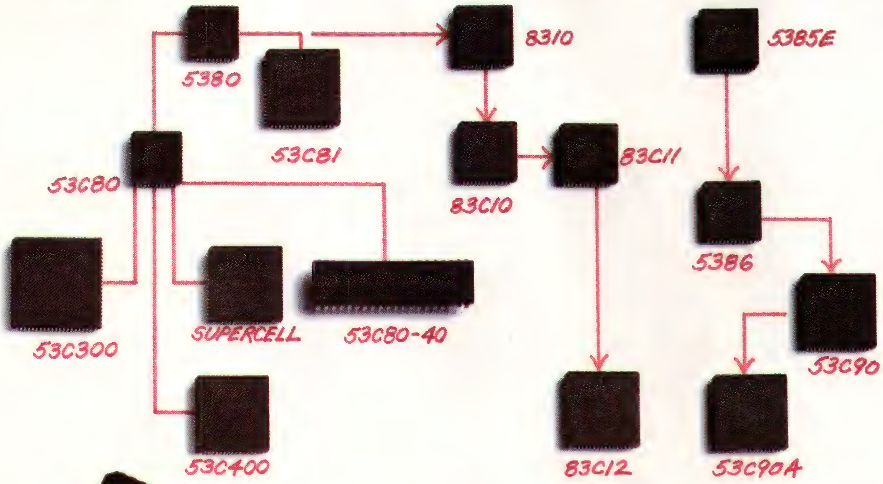
raising the for SCSI.



A big well-connected family.

Other suppliers can't show you much of a family tree compared to NCR. That's because NCR goes back to the "Mayflower" of SCSI controllers with the 5385 in 1982. The most recent offshoot of that original line is the high-performance 53C90A. Consistent with good family planning the software for the 53C90 is similar to our 5385 and 5386, so you can quickly convert to the 53C90. A single chip host bus adapter (53C400), integrated buffer controller (53C300) and an ASIC supercell fill out our product offering. And you can bet we'll be there when you need SCSI II.

How to get zap-resistance, latch-up protection and the blessings of the FCC.

For example, the NCR 5380 and 53C90 families give you ESD protection up to 10,000 volts on the SCSI bus. NCR also provides controlled fall times to reduce the undershoot that could cause other CMOS chips to latch-up. Controlled assertion rates also reduce generated RFI, an important factor in winning FCC approval for the final product.

It's time to raise your standards.

In SCSI, it's not so much if you implement the standard, but how. Because our chips have an edge over other chips from other manufacturers, they can help give you and your product an edge in the market. We've shipped more than 3-million 5385's and 5380's and production quantities of the 53C90. If you don't want to just settle for the standard, call NCR today.

For documentation call our hot line 1-800-334-5454. Or write to, NCR Microelectronics, SCSI Products, 1635 Aeroplaza Drive, Colorado Springs, CO 80916.

For technical assistance, call 800-525-2252, Telex 452457.

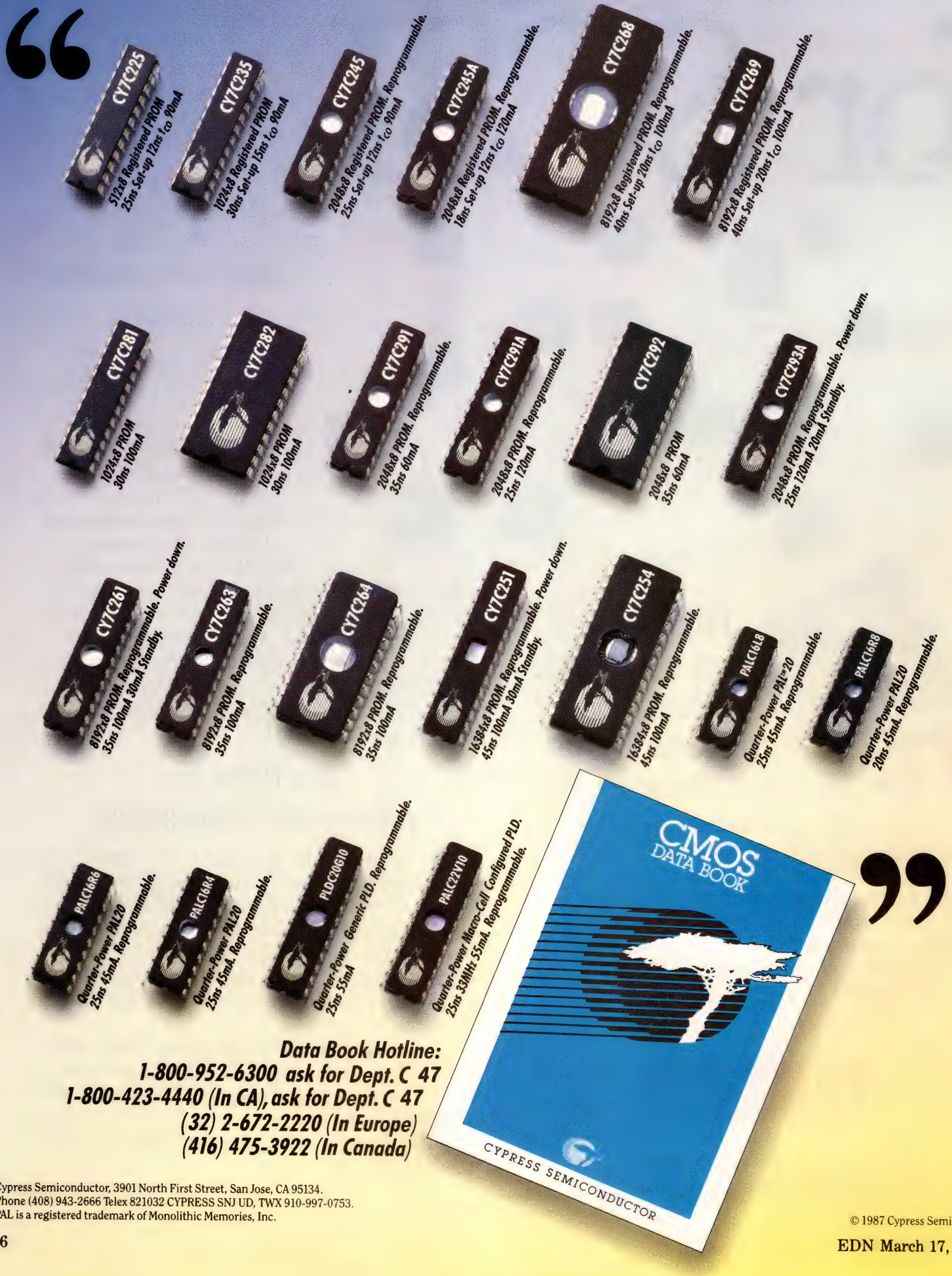
NCR

NCR Microelectronics Division

CIRCLE NO 32

No other PROM or PLD vendor can make this statement:

“



512x8 Registered PROM
25ns Set-up 12ns tco 90mA

1024x8 Registered PROM
30ns Set-up 15ns tco 90mA

2048x8 Registered PROM. Reprogrammable.
25ns Set-up 12ns tco 90mA

2048x8 Registered PROM. Reprogrammable.
18ns Set-up 12ns tco 120mA

8192x8 Registered PROM. Reprogrammable.
40ns Set-up 20ns tco 100mA

8192x8 Registered PROM. Reprogrammable.
40ns Set-up 20ns tco 100mA

1024x8 PROM
30ns 100mA

1024x8 PROM
30ns 100mA

2048x8 PROM. Reprogrammable.
35ns 60mA

2048x8 PROM. Reprogrammable.
25ns 120mA

2048x8 PROM
35ns 60mA

2048x8 PROM. Reprogrammable. Power down.
25ns 120mA 20mA Standby.

8192x8 PROM. Reprogrammable. Power down.
35ns 100mA 30mA Standby.

8192x8 PROM. Reprogrammable.
35ns 100mA

8192x8 PROM. Reprogrammable.
35ns 100mA

16384x8 PROM. Reprogrammable. Power down.
45ns 100mA 30mA Standby.

16384x8 PROM. Reprogrammable.
45ns 100mA

Quarter-Power PAL™20
25ns 45mA. Reprogrammable.

Quarter-Power PAL20
20ns 45mA. Reprogrammable.

Quarter-Power PAL20
25ns 45mA. Reprogrammable.

Quarter-Power PAL20
25ns 45mA. Reprogrammable.

Quarter-Power Generic PLD. Reprogrammable.
25ns 55mA

Quarter-Power Macro-Cell Configured PLD.
25ns 33MHz 55mA. Reprogrammable.

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EDITORIAL

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We continually rely on readers to provide our applications articles, which contain useful technical information that helps you do your job better. You can count on four or five of those articles in each issue. I'm sorry to say, though, that many people think writing for EDN is a formidable task. It's true that we're selective in what we publish, but we've made the writing task a bit less daunting. You can get a copy of our revised booklet *Writing for EDN* by calling (617) 558-4216 and giving us your name and mailing address, or you can circle number 800 on the Information Retrieval Service card bound in this issue.

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Jon Titus
Editor

Expand your

design vision.

Enhance your design at any stage with RCA CMOS 6805 micros and SPI peripherals.

Your challenge is to increase system performance and capability while reducing board size.

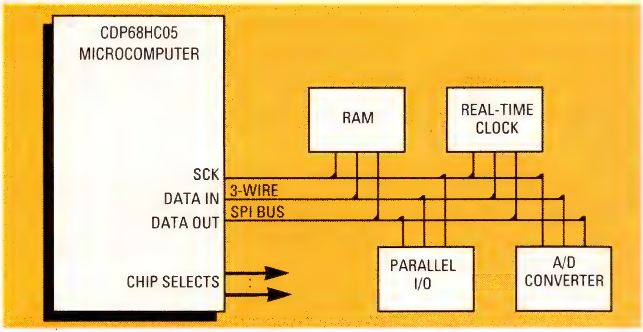
Not an easy job. But certainly easier when you use our 6805 and 68HC05 micros and serial peripheral interface devices.

Extend your micro's power.

Many microcomputers rely on parallel I/O ports to communicate with peripheral devices. An inefficient method at best.

That all changes with the serial peripheral interface incorporated into our 68HC05 microcomputers.

This three-wire (plus device select) synchronous, full-duplex, serial communication system contains separate lines for input and output data, serial clock and device select. You don't have to sacrifice I/O ports to communicate off-chip: our 68HC05 micros can communicate with our own serial peripherals, the serial peripherals of other manufacturers, and even with other microcomputers via only three port lines.



True design versatility.

The real beauty of the SPI is that it eliminates limitations imposed by microcomputers.

For example, you can easily extend the amount of I/O or memory with SPI RAMs, I/O chips or shift registers. And the modular SPI bus gives you the ability to expand without losing lots of PC-board space. Reduced package sizes and minimized interconnect wiring lead to reduced board size.

And since you don't need complex software to operate the bus, you save ROM space.

Right now, we can offer you a versatile family of peripheral devices, including 128-byte and 256-byte static RAMs, a real-time clock with RAM, an 8-bit programmable I/O port, and a 10-bit 8-channel A/D converter. And more parts are coming soon, including a digital pulse-width modulator and a serial bus interface chip for networking microcomputers. These serial peripherals are also compatible with other microcomputer types.

Powerful family of micros.

We can provide 6805 microprocessors for external memory address, but the heart of our SPI system is the 6805 Series high-speed CMOS microcomputers:

68HC05 Microcomputers

Features	**68HC05C4**	**68HC05C8**	**68HC05D2**	**68HC05D2A**
Pins	40	40	40	28
On-Chip RAM (bytes)	176	176	96	96
On-Chip User ROM (bytes)	4160	7744	2176	2176
Bidirectional I/O Lines	24	24	28	16
Unidirectional I/O Lines	7 inputs	7 inputs	3 inputs	3 inputs
Timer size (bits)	16	16	16	16
Prescaler size (bits)	*	*	*	*
External timer oscillator	no	no	yes	yes
Serial peripheral interface	yes	yes	yes	no
Serial communications interface	yes	yes	no	no

*prescaler fixed as ÷4

Easy to prototype, too.

If you need another reason to choose our 6805 family, here it is: they're so easy to prototype with our Piggyback! We have the 68EM05C4 and 68EM05D2 Emulators, custom 40-pin packages that contain the C4/C8 or D2 micros with a Piggyback EPROM socket.

When installed with a 27C64 EPROM, these devices together become functionally identical to a CDP68HC05C4, CDP68HC05C8 or CDP68HC05D2.

Two final points: we'll give you fast turnaround, and a wide variety of packages.

For more information, call toll-free 800-443-7364, extension 22. Or contact your local GE Solid State sales office or distributor.

In Europe, call: Brussels, (02) 246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm, (08) 793-9500.

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Three great brands. One leading-edge company.

How to improve your designs by the process of elimination.

Here are five new ways to enhance your product's performance, or reduce costs, either by eliminating non-essential component features or by eliminating manufacturing steps with ready-made subassemblies.

Long-life miniature pushbuttons provide wide-angle viewing, $1 each.

Our special, low-cost square and rectangular MML pushbuttons feature simple momentary action, and come in a choice of five button colors. They're ideal for applications that require high performance, but not UL listing or audible feedback.

Square buttons are available in LED or incandescent lighted versions with one-piece molded lens caps for good visibility from any angle. All versions are covered by an 18-month warranty, and come at a defect rate of less than 50 per million. Actual sizes, .39″ x .39″ square, .39″ x .59″ rectangular. All are .67″ deep. **CIRCLE NO 147**

High-resolution gear tooth sensor has built-in magnets and resistors to simplify design and installation.

The completely self-contained SR7P gear tooth sensor reduces manufacturing steps by providing a magnetoresistive sensing element, biasing magnet, signal-conditioning electronics and pull-up resistor in a compact thermoplastic housing with plug-in connector.

Operating on a standard 5 VDC power supply, the sensor can detect ferrous targets as small as 32 teeth/inch, with digital current sinking output throughout a speed range of 0-12 kHz. Actual size, .345″ x 1.25″ x 1.775″. **CIRCLE NO 148**

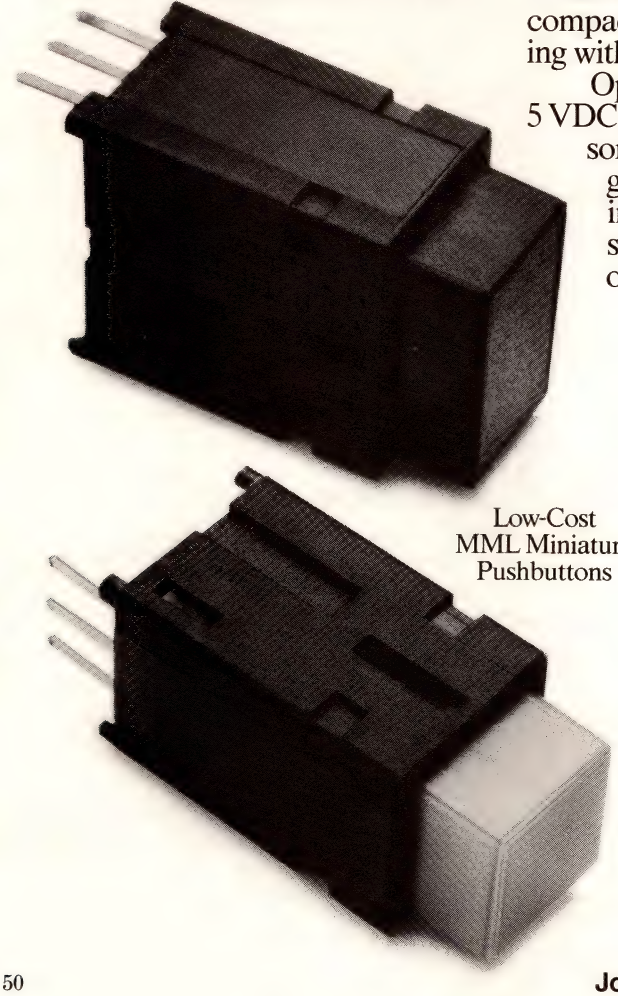
Simple cantilever spring switch saves money where precision snap-action isn't needed.

Our V10 Series basic switch uses a cantilever spring system that's ideal for simple on/off applications, or where its spring rate, travel or force specifications are more compatible with your requirements. The V10 comes in general purpose and UL/CSA versions, with a wide choice of plunger or integral lever actuators, and capacities from 1 to 25 amps at 277 VAC.

All V10s feature combination quick-connect/solder terminals that are compatible with industry standard receptacles and connector blocks. Actual size .63″ x .40″ x 1.14″. **CIRCLE NO 149**

In-line digital current sensor eliminates the need for an external conductor.

Now there's a way to monitor uninterruptible power supplies without sacrificing precious board space. Our miniature CS series-connect current sensor

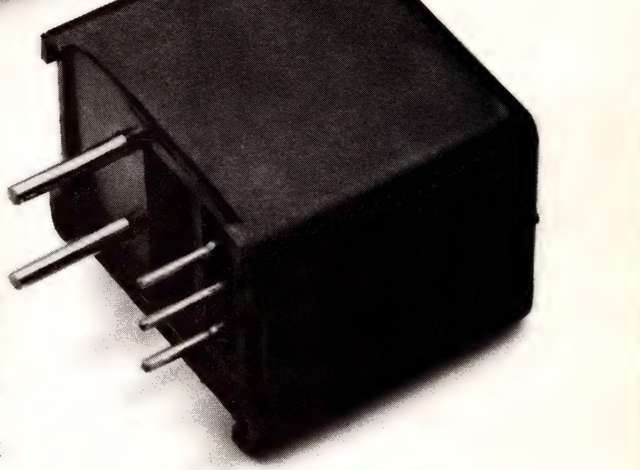


Low-Cost
MML Miniature
Pushbuttons

SR7P High-Resolution
Gear Tooth Sensor

Join us at Electro, May 10; Booth 642

V10 Non-Snap
Basic Switch



CS Series-Connect
Digital Current Sensor

can be mounted directly to a PC board. It uses a Hall effect chip to respond accurately within ±10% of a setpoint between 1.3 and 15 amps. Digital output is compatible with electronic control devices. Actual size, .58″ x .50″ x .67″.
CIRCLE NO 150

Ergonomic pushbutton subassemblies increase design freedom, reduce manufacturing steps.

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Please gather the signatures of your colleagues who belong to the IEEE. Return the petitions to the address shown below.

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Name (print)	*Name (sign)*	*Member Number (if known)*	*Date*

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MULTIBUS II
TAKES YOU
BACK TO
THE BASICS

. . . AND INTO THE FUT

MULTIBUS II OPENS UP ADVANCED APPLICATIONS IN WAYS NO OTHER BUS CAN.

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An inherently more reliable bus, suitable for applications that process huge volumes of data at unprecedented speeds.

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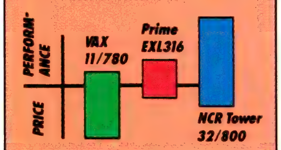
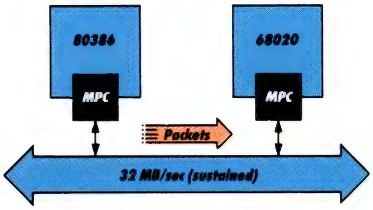
A new generation of microcomputer systems based on Multibus II is now emerging, to redefine standards of price and performance.





BASIC #2: HARDWARE-ASSISTED MESSAGE PASSING.
This advanced technique gives Multibus II a true sustained bandwidth of 32 megabytes per second. Standardized in a single silicon chip, message passing simplifies sytem design, and makes it possible to mix totally different microprocessor architectures and operating systems in the same application.

A more maintainable bus, to reduce the cost and complexity of configuration, trouble-shooting and repair.

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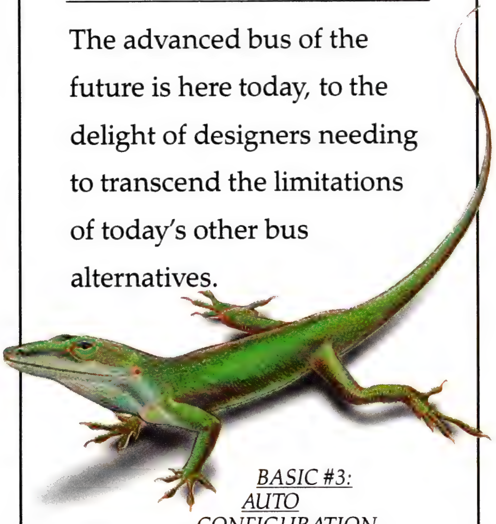
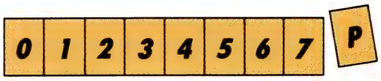


BASIC #3: AUTO CONFIGURATION.
Like a chameleon, Multibus II boards automatically configure themselves when system power is turned on, eliminating DIP switch hassles during configuration and maintenance.



BASIC #1: PARITY.
Multibus II's parity error detection provides the basic protection needed by advanced applications that process large volumes of data at high speeds.

For example, NCR and Prime based their newest Tower™ and EXL™ systems on Multibus II. Both provide several times the power of a VAX™ 11/780 minicomputer,

TRADITIONAL VS. A

	CHARACTERISTICS	TRADITIO MULTIBUS I
BASIC FEATURES	TIMING (Synchronous or Asynch)	ASYNCH
	PIN USAGE (MPX) Multiplexed (NON) Non-Multiplexed	NON
	ARBITRATION (CENT)ralized (DIST)ributed	CENT.
	INTERRUPTS (DED)icated (VIR)tual	DED.
	GLOBAL MEMORY Communications	YES
ADVANCED FEATURES	PARITY	NO
	AUTO-CONFIGURATION (Geographic Addresses)	NO
	MESSAGE PASSING (Hardware)	NO
	BUS I/F SILICON	NO
OTHER FEATURES	ADDRESS WIDTH (Bits)	20,24
	DATA WIDTH	8,16
	BOARD AREA (sq. in.)	84
	CONNECTOR TYPE	EDGE
	MAX. 5V POWER (Per slot)	24A

*Implemented outside IEEE 1014 using several proprietary schemes.

at a fraction of the price.

A major U.S. department store chain has put into operation a revolutionary home shopping network, based on Multibus II.

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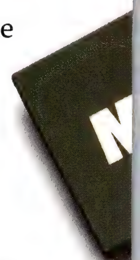
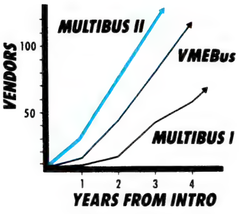


URE.



MULTIBUS II:
The world's fastest growing open system architecture!

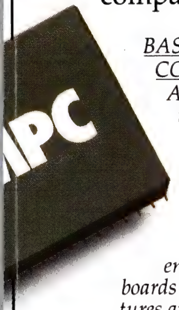
architecture for the future for advanced factory automation applications.

And two leading aerospace companies are using Multibus II to build the world's most advanced aircraft flight simulators.

Throughout the world, these and scores of other companies have introduced

VANCED ARCHITECTURES

AL BUSES	**ADVANCED BUSES**	
VME	**MULTIBUS II**	**VAX BI**
ASYNCH	SYNCH	SYNCH
NON	MPX	MPX
CENT.	DIST.	DIST.
DED.	VIR.	VIR
YES	YES	YES
NO	YES	YES
NO	YES	YES
NO*	YES	YES
AVAIL. '88	YES	YES
24,32	32	32
8,16,24,32	8,16,24,32	8,16,24,32
59.8	80	73.4
DIN	DIN	ZIF
6A	15A	Not Published



BASIC #4: MULTI-VENDOR COMPATIBILITY.
A host of unique features ensure that Multibus II boards will work together efficiently and dependably. The IEEE 1296 specification is complete and concise. And, the Multibus II Message Passing Coprocessor (MPC), now universally available, ensures compatibility even between boards using different processor architectures and operating system software.

or are now developing Multibus II applications that set new standards of performance, price and reliability.

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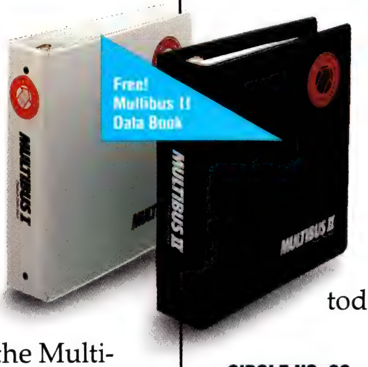
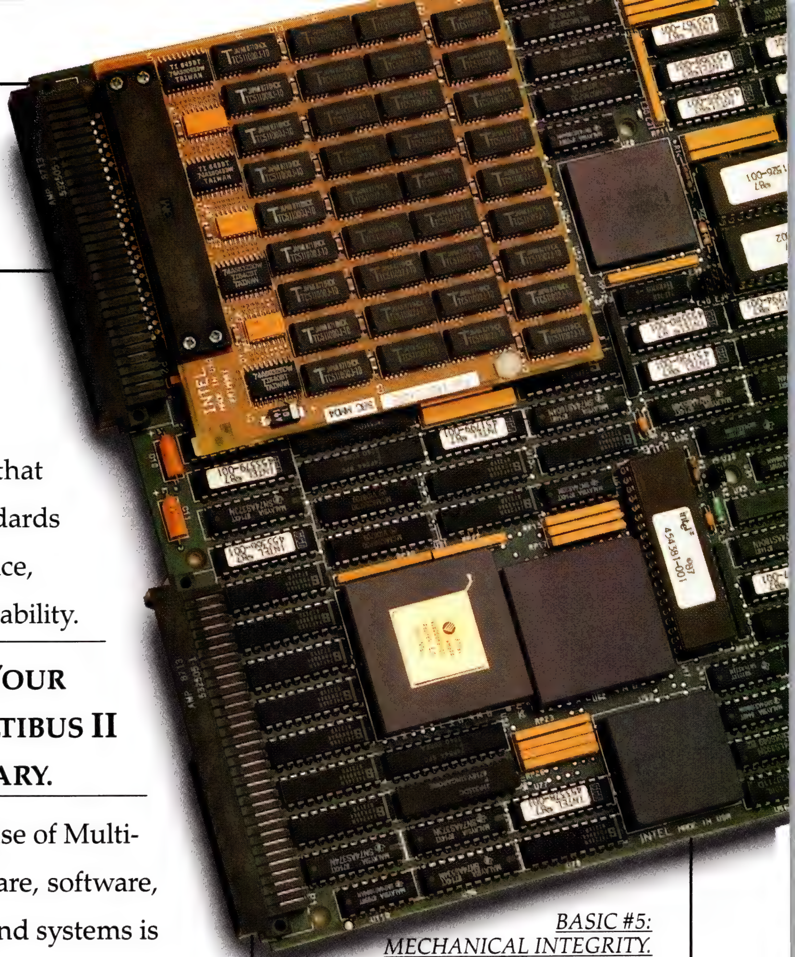


And, to keep your Multibus II library organized, the Multibus Manufacturers Group will send you this convenient indexed bookshelf binder. Absolutely free!



BASIC #5: MECHANICAL INTEGRITY.
Naturally, Multibus II uses DIN connectors, for the most reliable mechanical connections. But, it also incorporates built-in front panels for EMI shielding. And, its standard Eurocard form factor provides enough board space (a full 80 sq. in.) to accommodate complex designs.

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intel®	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 (800) 548-4725	•	•	•		•	•	•	•	•	•	•
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MICROBAR SYSTEMS, INC.	785 Lucerne Drive Sunnyvale, CA 94086 Contact: Bill Burton Telephone (408) 720-9300 FAX (408) 773-9475	•			•		•			•		•
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Pioneering engineers begin to adopt board-level automatic test generation

KEEPING AMERICA COMPETITIVE

Dan Strassberg,
Associate Editor

You can recognize a pioneer by the arrow in his back: Despite that adage's implied warning, some designers of board-level products are beginning to adopt design methodologies compatible with testability techniques like automatic test-pattern generation (ATPG).

These pioneers might well acquire a few surface wounds. But proponents of design for testability, or DFT (see **box,** "Overcoming the initial problem"), maintain that companies that delay or avoid confronting testability at the design stage risk much more serious—and possibly even fatal—injury.

In its most elemental form, DFT yields designs that are partitioned by function, that can be easily initialized and controlled, and whose behavior can be observed. Some people, however, use the term DFT to imply considerably more.

For example, DFT approaches include such highly formalized design techniques as LSSD (level-sensitive scan design), one of several scan-design methodologies. With the exception of boundary scan, which is a technique for isolating functional blocks and observing them at their I/O terminals, scan design enables you during test to reconnect sequential logic (which most ATPG programs can't handle) to form combinatorial networks (which ATPG programs can handle).

This board test system, *Hewlett-Packard's 3065ST, performs digital in-circuit and analog-functional tests. An automatic program generator for it runs on the vendor's workstations.*

DFT will change attitudes

Test vectors, also called test patterns, are the combinations of 1s and 0s that a tester applies and looks for when it tests a logic net. Although adherence to DFT approaches in their simplest form doesn't guarantee success in generating vectors automatically, it improves the chances of success and can significantly reduce test-development time, even with manual vector generation. To achieve its goals, DFT imposes new disciplines on designers and requires them to reorient their priorities. DFT advocates insist that new attitudes are mandatory—they insist that tried-and-true approaches (for example, a design engineer's treating test as someone else's problem) simply won't work in today's market.

Many factors influence the pace at which companies are adopting DFT and ATPG, particularly for board-level designs. Although ATPG and DFT have not yet taken device design by storm, these techniques have so far affected the design of ASICs and PLDs much more than they have that of board-level products (**Ref 1**).

Despite offering solutions to very real and pressing problems, vendors of ATPG software and other test-development aids recognize that if they want to grow they must deal with several legitimate concerns. They must also educate their potential customers and thus dispel a long list of misconceptions. Here are some of the issues they are addressing:

- Greater complexity of boards than of ICs
- The perception that ASIC design is risky enough to justify unusual approaches, but board-level design is not
- Difficulty in measuring costs

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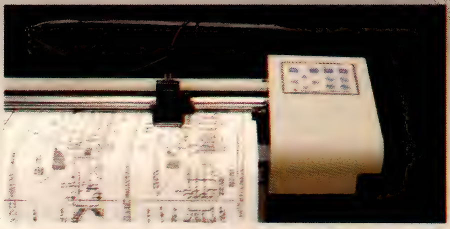

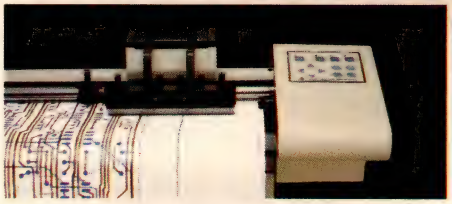

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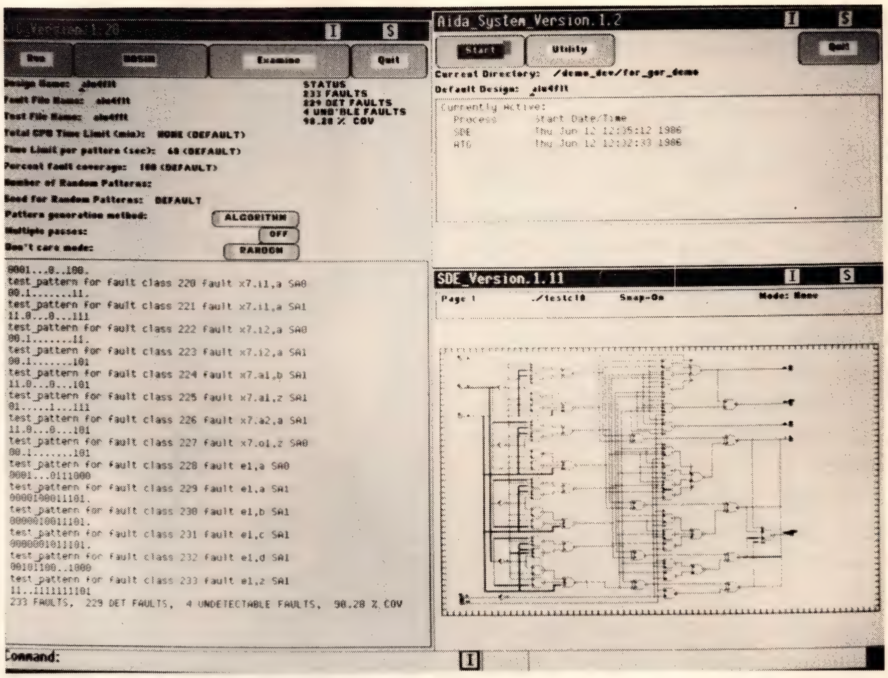
CIRCLE NO 35

of current test and test-development practices

- Use of traditional methods, because some companies don't understand the shortcomings of current methods and so they feel comfortable with them
- Cost of learning how to apply new techniques
- Cost of computing resources required to run ATPG software
- Fear of requiring more pc-board real estate
- Fear of higher component cost
- Fear of lower reliability
- Slow adoption of logic simulation
- Incompatibilities of simulator/ATPG-database formats
- Incompatibility between automatically generated vectors and tester capabilities
- Difficulty in obtaining scannable components.



```
Design Name:  alu4flt
Fault File Name:  alu4flt
Test File Name:  alu4flt
Total CPU Time Limit (min):  NONE (DEFAULT)
Time Limit per pattern (sec):  60 (DEFAULT)
Percent fault coverage:  100 (DEFAULT)
Number of Random Patterns:
Seed for Random Patterns:  DEFAULT
Pattern generation method:        ALGORITHM
Multiple passes:                  OFF
Don't care mode:                  RANDOM

STATUS
233 FAULTS
229 DET FAULTS
4 UND'BLE FAULTS
98.28 % COV
```

```
0001...0..100.
test_pattern for fault class 220 fault x7.i1,a SA0
00.1.......11.
test_pattern for fault class 221 fault x7.i1,a SA1
11.0...0...111
test_pattern for fault class 222 fault x7.i2,a SA0
00.1.......11.
test_pattern for fault class 223 fault x7.i2,a SA1
00.1.......101
test_pattern for fault class 224 fault x7.a1,b SA1
11.0...0...101
test_pattern for fault class 225 fault x7.a1,z SA1
01.....1...111
test_pattern for fault class 226 fault x7.a2,a SA1
11.0...0...101
test_pattern for fault class 227 fault x7.o1,z SA0
00.1.......101
test_pattern for fault class 228 fault e1,a SA0
0001...0111000
test_pattern for fault class 229 fault e1,a SA1
000010001101.
test_pattern for fault class 230 fault e1,b SA1
0000010011101.
test_pattern for fault class 231 fault e1,c SA1
00000001011101.
test_pattern for fault class 232 fault e1,d SA1
00101100..1000
test_pattern for fault class 233 fault e1,z SA1
11..1111111101
233 FAULTS,  229 DET FAULTS,  4 UNDETECTABLE FAULTS,  98.28 % COV

Command:
```

```
Current Directory:  /demo_dev/for_gor_demo
Default Design:  alu4flt
Currently Active:
  Process       Start Date/Time
  SDE           Thu Jun 12 12:35:12 1986
  ATG           Thu Jun 12 12:32:33 1986
```

```
Page 1          ./testc10       Snap-On                 Mode: None
```

***Multiple windows on a workstation screen** allow you to view your schematic as well as the descriptions of vectors generated by Aida Corp's ATPG.*

Big boards challenge ATPG

Although ASICs and PLDs are complex, with gate counts in the neighborhood of 10,000, they tend to be significantly less so than the typical logic board designed with CAE tools. Such boards—especially if they house complex chips—can easily contain more than 100,000 gate equivalents. The diversity and complexity of board-level designs taxes many of today's ATPG programs beyond their limits. But if you design in partitionable functional blocks, you can frequently use ATPG on networks that at first glance seem to exceed the capabilities of the software.

Board-level test-development procedures evolved at most equipment-manufacturing companies before board complexity approached today's levels. Many of these companies have little idea of the cost of developing or performing board-level tests, and their managements have not yet recognized the inadequacy of the classical approaches they are using. Naturally, if they are unaware of the shortcomings of existing practices, managers can see no reason to make changes.

Overcoming the initial problem

The electronics industry has its share of confusing acronyms and abbreviations, but few seem quite so unfortunate as DFT—used throughout this article, and throughout the industry, to mean design for testability. Practically everyone who refers to design for testability as DFT uses those same initials to denote digital functional test and sometimes dynamic (as opposed to static) functional test, a subset of digital functional test. To an even larger group of EEs, DFT means discrete Fourier transform. It's quite likely that someone reading this article is planning to employ DFT to test a high-speed signal-processing board that performs DFTs, and because of the board's complexity, he plans to make DFT a guiding principle in his project. Of course, his pc (printed-circuit) vendor probably uses PCs (personal computers) for both PC (process control) and PC (production control). Now, is that perfectly clear?

But unlike printed circuits, ASICs are a new technology—one which engineers and managers realized warranted a complete set of new tools. These tools now exist, and ironically, are ready to be applied to the older, pc-design technology, if only engineers and managers realize the techniques' potential.

ATPG minimizes ASIC risk

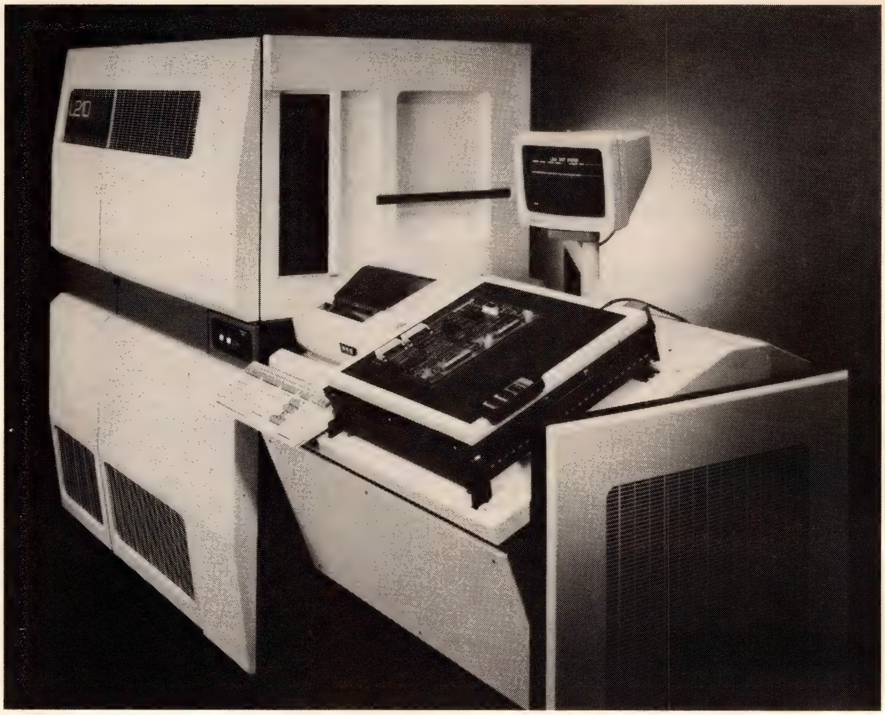
When you develop ASICs, you spend a lot of money up front, and you wait a long time to see real devices. If prototypes don't work, you can't probe their internal nodes and you can't make repairs. Because of these risks, many companies perceive that IC development warrants extraordinary measures and are willing to try using ATPG on their custom chips. With printed boards, the situation is—or appears to be—different, so many of the same companies are unwilling to apply ATPG to their board-level designs.

Much of the automated test generation for ASICs occurs as an offshoot of logic and timing simulation, which are part of the ASIC design phase. The patterns generated are for design verification; they tell a designer primarily whether his design will do what he intended it to—assuming that the manufacturing process hasn't introduced any defects.

At best, such pattern sets provide an incomplete solution for production test or incoming inspection. In fact, some CAE-software vendors insist that you only cause confusion if you use the term ATPG to refer to development of test patterns for design verification. They say that you should use ATPG only to describe the generation of vectors for determining whether manufacturing has introduced defects. (Sometimes such vectors also locate the defects.)

If you use design-verification test patterns in production board test, you can miss faults introduced during board-loading and soldering, and you can waste time checking device properties that you should have checked before you loaded the devices onto the board. But although design-verification patterns are usually inadequate for production test, the converse isn't true. You don't develop production test vectors to find functionality problems in boards without manufacturing-induced faults, but vectors developed for production test frequently reveal problems that design verification should have uncovered.

Another factor inhibiting adoption of ATPG is the slow pace of acceptance of logic simulation itself. If you wanted to use ATPG to generate a board's test vectors, you would almost certainly design the board using simulation; otherwise you would have to create the equivalent of the simulation database from scratch. So far, even for complex boards, use of logic simulation remains in its infancy.



Exemplifying large ATE systems *capable of performing both in-circuit and functional testing, Teradyne's L210 combinational board test system employs high-speed pin electronics to help it diagnose timing faults.*

The cost of most ATPG software is not insignificant **(Table 1)**. But some potential customers worry about having to commit great sums for computer resources (CPUs, data-storage hardware, and workstations) to run ATPG programs. For companies using simulation, however, the resources may cost nothing—at least at first. Usually, there's no need to augment a computer system until you are utilizing it fully. On the other hand, if you didn't originally factor ATPG into your plans but are now using it, you may have to acquire additional computer equipment sooner than you had expected to. To the relief of engineers concerned with controlling the cost of individual projects, most companies recognize that such equipment is used on many projects and is part of the cost of being in business; rarely do they assign the charges to a single development program.

Fear of the unknown as well as engineers' innate conservatism affects their willingness to make changes. In the case of DFT, managements fear that the time designers spend in learning how to apply the new techniques will add to project costs and slow down product-development schedules. Something to keep in mind is that an organization normally needs to climb the DFT learning curve only once—not once per project. After engineers have learned the techniques, the organization reaps additional benefits with each new project.

Designers fear that testable designs will require more printed-circuit real estate and have higher parts cost and possibly lower reliability than equivalent "untestable" designs. Of these concerns, the one about reliability is easiest to disprove: With appropriate components, the added complexity of a scannable design (measured by gate count) is usually less than 10%. A cost attributable to the added complexity is an estimated 10% decrease in MTBF (mean time between failure); but a benefit is an

It's not obvious because the STD BUS is usually hidden away, controlling your tollways, the temperature of your office, the quality of your manufacturing, and even the animation in the local fun park.

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PL057

CIRCLE NO 36

estimated order-of-magnitude reduction in MTTR (mean time to repair).

MTTR is usually a small fraction (less than about 1%) of MTBF. Suppose an untestable product has an MTBF of 1000 hours and an MTTR of 10 hours: Its availability is 100(1000−10)/1000, or 99%. If the

TABLE 1—REPRESENTATIVE BOARD- AND DEVICE-LEVEL TESTABILITY PRODUCTS

VENDOR	PRODUCT	DESCRIPTION	PREREQUISITES	US BASE PRICE
AIDA CORP	AIDA ATPG	GENERATES PATTERNS WITH 100% COVERAGE OF DETECTABLE FAULTS IN SCANNABLE DESIGNS. USES PATH-SENSITIZING AND RANDOM-VECTOR GENERATION. DETECTS "STUCK-AT" FAULTS. SUPPORTS BIDIRECTIONAL I/O AND 3-STATE BUSES AS WELL AS WIRED-OR AND WIRED-AND GATES.	APOLLO OR SUN WORKSTATION AND AIDA FAULT SIMULATOR	$45,000 (AIDA FAULT SIMULATOR: $15,000)
ANVIL SOFTWARE	ANVIL ATG SOFTWARE	GENERATES FUNCTIONAL TESTS FOR PROGRAMMABLE LOGIC DEVICES WITHOUT USING PRELOAD. SUPPORTS >50 DEVICE TYPES. LINKS TO COMPONENT AND IN-CIRCUIT TESTERS.	IBM PC OR COMPATIBLE WITH 640k-BYTE RAM AND HARD DISK	$4950
GATEWAY DESIGN AUTOMATION CORP	TESTSCAN	ATPG FOR DIGITAL CIRCUITS EMPLOYING SCAN-DESIGN. PROVIDES 100% TEST-VECTOR COVERAGE, DESIGN-RULE AUDIT, AND FAULT SIMULATION. SUPPORTS SCAN-PATH, LSSD, RANDOM-ACCESS SCAN, AND SCAN-SET TECHNIQUES.	IBM, APOLLO, SUN, OR VAX/VMS	$75,000
	BITGRADE	FAULT SIMULATOR AND RANDOM-VECTOR GENERATOR FOR CIRCUITS WITH BUILT-IN SELF-TEST (BIST) ABILITY. INCLUDES HARDWARE-DESCRIPTION LANGUAGE.	IBM, APOLLO, SUN, OR VAX/VMS	$25,000
GENRAD INC	GENESIS	TEST PROGRAMMING ENVIRONMENT FOR GR 275X SERIES OF HIGH-PERFORMANCE BOARD-TEST SYSTEMS. GENERATES MULTISTRATEGY (IN-CIRCUIT/FUNCTIONAL) TEST PLANS. RUNS IN TESTER OR OFF-LINE IN WORKSTATION.	SUN WORKSTATIONS WITH SUN UNIX	INCLUDED IN PRICE OF TEST SYSTEM; NOT AVAILABLE SEPARATELY
	ATG-32	TEST-GENERATION SOFTWARE FOR GR 227X FAMILY OF MID-RANGE COMBINATIONAL TESTERS. RUNS OFF-LINE. DOWNLOADS PATTERNS VIA ETHERNET/GRNET NETWORK.	ANY DEC VAX SYSTEM OR GENRAD 3200V	$30,000
HEWLETT-PACKARD CO	HP 74241A	AUTOMATICALLY GENERATES READY-TO-RUN IN-CIRCUIT ASIC- AND FUNCTIONAL CIRCUIT-TEST PROGRAMS THAT ARE FULLY COMPATIBLE WITH HP-3065 SERIES TESTERS.	HP ELECTRONIC DESIGN SYSTEM; HP 3065-SERIES TESTER.	$3980
HHB SYSTEMS INC	THESEUS	ANALYSIS TOOL THAT PINPOINTS AREAS NEEDING IMPROVED TESTABILITY. ASSURES THAT VECTORS PROVIDE GOOD FAULT COVERAGE. HANDLES DESIGNS USING SEQUENTIAL DEVICES, FEEDBACK LOOPS, AND RECONVERGENT FANOUT.	DEC VAX/VMS OR SUN/UNIX, WITH 8M BYTES RAM AND 300M-BYTE HARD DISK.	$100,000
LOGICAL SOLUTIONS TECHNOLOGY INC	TESTABILITY CHIP SET	TESTABLE FUNCTIONAL CIRCUITS (SHIFT REGISTERS, LATCHES, DECODERS, ETC) THAT PROVIDE PERFORMANCE PLUS A TESTABILITY-BUS PORT. COMMERCIAL AND MIL, LEADED AND SURFACE-MOUNTING VERSIONS.	NONE	$6 TO $50 (100)
NCR CORP	VITEST	FACILITATES DEVELOPMENT OF HIGH-SPEED TEST PROGRAMS TO RUN ON TRILLIUM AND SCHLUMBERGER SENTRY DEVICE TESTERS. CHECKS PATTERN TIMING AND BUS CONTENTION. USES BEST- AND WORST-CASE SIMULATIONS TO ANALYZE PATTERNS. IDENTIFIES POSSIBLE FUNCTION ERRORS.	CADNETIX, DAISY, MENTOR GRAPHICS, OR VALID WORKSTATIONS, OR DEC VAX MAINFRAMES	INCLUDED AS PART OF VENDOR'S VISYS ASIC-VERIFICATION PACKAGE. VISYS: $7950
SILICON COMPILER SYSTEMS INC	AUTOMATIC TEST GENERATION (ATG)	SET OF SOFTWARE TOOLS THAT EVALUATES TESTABILITY OF BLOCKS, MODULES, AND CHIPS; GENERATES COMPRESSED TEST VECTORS; AND DETERMINES GATE-LEVEL TEST COVERAGE OF THE VECTORS.	GENESIL DESIGN SYSTEM + APOLLO DN3000, DN4000, DN570T; SUN 3; OR DEC VAX 8650 OR μVAX2.	$39,500 PER USER
TERADYNE INC	CIRCUIT BREAKER	ACHIEVES >95% COVERAGE OF LOGIC AND FUSE FAULTS; CREATES GRADED DYNAMIC TESTS FOR SLOW-PATH FAULTS ON COMBINATIONAL AND HIGHLY SEQUENTIAL PLDs. FOR HIGH-VOLUME INCOMING INSPECTION AND IN-CIRCUIT BOARD TEST.	LASAR VERSION 6 SIMULATION SYSTEM RUNNING ON ANY VAX/VMS SYSTEM.	$6250 FOR VAXSTATION 2000, $70,000 FOR VAX 8800
TEST SYSTEMS STRATEGIES INC	TEST DEVELOPMENT SERIES (TDS)	TEAMS UP ASIC-DESIGN AND SIMULATION TOOLS TO PRODUCE SETS OF FUNCTIONAL VECTORS FOR SPECIFIC ATE FORMATS. SUPPORTS >30 TESTER TYPES FROM EIGHT VENDORS AND 14 SIMULATION ENVIRONMENTS.	APOLLO/AEGIS, SUN/UNIX, OR DEC VAX/VMS	$28,000 (DEPENDS ON SIMULATOR AND TESTER)

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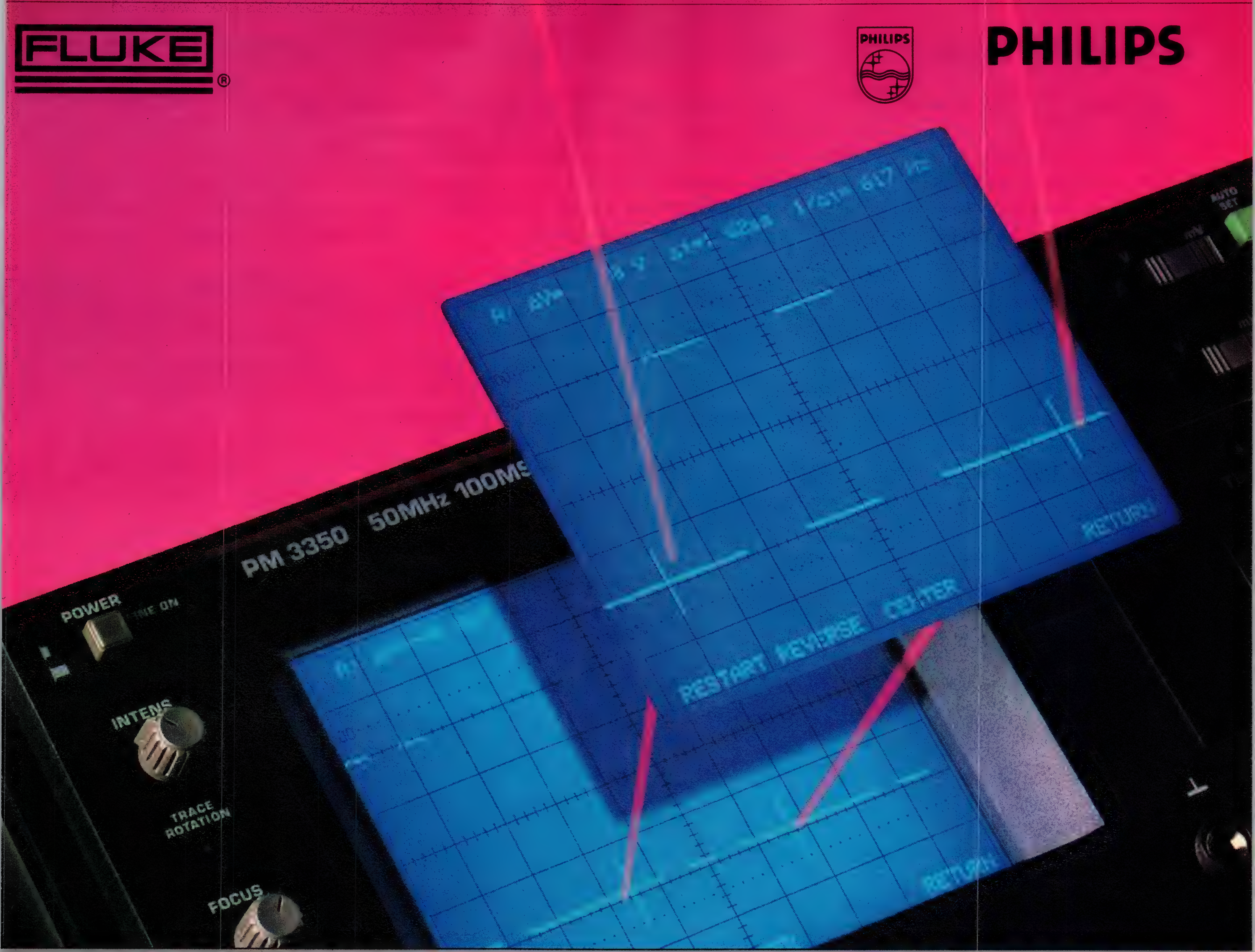

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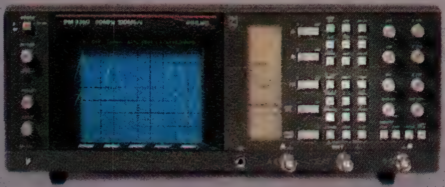

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equivalent testable product has an MTBF of 900 hours and an MTTR of one hour, its availability is 99.89%. The testable product is unavailable 0.11% of the time, only ⅓ as much as the untestable product. Chances are the customer is *really* concerned more about being able to use the product than he is about its failure rate. Quicker repair is a key reason why field-service groups are becoming firm believers in DFT.

DFT can reduce MTTR if, for example, in a large system containing dozens of boards, you can isolate faults to the board level by connecting a portable tester to "testability connectors" accessible from the

Board test strategies: The bus is waiting

When you use ATE to test a loaded pc board, the testing can fall into two major categories or into combinations of the two. The categories are in-circuit and functional. Until about five years ago, board-test systems were characterized by which of these two types of testing they performed. Now, so-called combinational systems are commonplace. The word "combinational" really has nothing to do with combinational logic, although a combinational tester clearly can test combinational logic. As used by the ATE manufacturers, the word refers to the systems' *combination* of functional and in-circuit test capabilities.

With in-circuit testing, you basically test the components *after* they have been loaded onto the board to prove that the assembly process hasn't damaged them. In-circuit testing is popular because, compared with functional testing, test programs are easy to write, and they inherently isolate defective components.

A tester can perform in-circuit tests on a component even though the outputs of other components are connected to some of its pins. The tester accomplishes this feat by "back driving" the pins of the other devices. Suppose you are testing a gate whose input is driven low by the output of a flip-flop. If for a very brief interval, you force enough current into the node, you can make the output of the flip-flop go high, without, you hope, causing permanent damage.

In-circuit test has problems

But in-circuit testing has problems, too. One problem is that military agencies are unwilling to accept the idea that back driving doesn't introduce latent defects that cause components to fail prematurely, long after a board leaves the factory. A second problem relates to the effect of capacitive loading imposed by the tester on the circuit nodes of the board under test. A third problem results from the physical means used to access the component under test; the customary probing method uses bed-of-nails fixtures.

The trend toward surface-mount technology, with its high circuit densities, multiplies problems with bed-of-nails fixturing. When component leads are on 0.1-in. centers, the spring-loaded pogo pins used in bed-of-nails fixtures can be relatively durable. But pogo pins for the 0.50-in. centers, which are common with surface mounting, are much less durable, and when you surface-mount components on both sides of a board, you need still more complex and finicky clam-shell fixtures. Furthermore, pressing on the leads of surface-mount components (which don't pass through holes in a pc board) can cause bad solder joints to test good. Consequently, when laying out surface-mount boards that will be tested on in-circuit testers, printed-circuit designers now usually use probe points separate from the component leads and place them on 0.1-in. centers. Adding such probe points decreases component density to achieve testability.

In-circuit and SMT mix poorly

It isn't hard to see that if every surface-mounted component requires probe points on 0.1-in. centers, the density advantage of surface mounting quickly evaporates. The fight to retain high densities is one factor that has helped to bring about a resurgence of interest in functional testing. Functional testing actually attempts to make a board perform as it would in its target system. In true functional testing, you access the board only through its I/O connections, although you can add I/O connections to improve observability or controllability.

As mentioned earlier, it is much harder to write functional test programs than in-circuit programs, and functional programs don't inherently isolate faults. ATPG programs address both of these functional-testing problems. They can check a design for compliance with testability rules (for example, absence of asynchronous circuits, ability to break feedback loops by use of gates included for testability, and ability to substitute external clocks for internal ones that you can disable while testing). ATPG programs also perform "fault grading."

Like so many other terms in the digital-test front of the boards—the same connectors used to access the boards during production test (see **box,** "Board test strategies: The bus is waiting"). You should be able to control the boards and observe their function at these connectors, and so run functional tests of all the boards without unplugging them.

A more advanced (but much more costly) approach builds each board's control and observation points onto a connector that mates with the system backplane. The system itself contains the equivalent of the portable tester. With such capabilities, the system can diagnose its own faults; an operator's only function is

lexicon, fault-grading seems to be a misnomer; a better term would be pattern grading. Fault grading introduces simulated faults into a circuit model. The objective is to determine which faults a test pattern can find. Not only does fault grading let you evaluate the usefulness of particular patterns, it helps you to isolate faults by indicating which patterns detect them. Even though nodes stuck at 1 and stuck at 0 aren't the only possible faults (for example, nodes can be shorted together by a solder bridge), many years of experience have shown that you can get the information you need if you limit the simulated conditions to "stuck-at" faults.

Cluster testing holds answers

A promising approach to board test is called cluster-functional testing. It literally represents a divide-and-conquer strategy. The time required to write a functional test program appears to increase geometrically with the complexity of the circuit. By dividing a board into clusters—small blocks of logic that perform identifiable functions that you can isolate and test functionally—you reduce the test-development time significantly and improve the odds that ATPG will work. Moreover, compared with in-circuit testing, you dramatically reduce the number of probe points you need.

But cluster functional testing still usually presupposes that you probe the board with a bed-of-nails fixture. Testers without such fixtures can be more compact and less expensive than those based on the bed-of-nails approach. Here's where the IEEE testability bus enters the picture. The proposed standard (currently called P1149) is one of several that aim to simplify control and observation of logic—from the device level to the system level. In a board-level design that complied with the testability-bus standard, you would, if possible, place all control and observation nodes on connectors; but if a board lacks room for connectors, the standard allows node access via probe points.

An IEEE committee has been working on P1149 for several years and is ready to submit a formal proposal for acceptance. Despite sweeping goals, the committee feels the proposed standard is workable. It defines a set of testability inputs and outputs that should appear on every complying device, board, and system. As the complexity of the item increases, the number of testability inputs and outputs can increase. Implementation of the standard on an IC usually requires some dedicated pins.

At the board level, the standard recommends using dedicated pins on existing connectors, but if backplane pins are limited, you can substitute special test connectors. If space along the front of a board is at a premium, the test connectors can be accessible only if you place the board on an extender, and if there is no room for test connectors at all, you can use probe points. Using backplane pins provides the greatest potential advantage; test connectors accessible without extending boards are next best, and so on.

Bye bye, bed of nails?

By eliminating bed-of-nails fixturing in most cases, the testability bus appears to make it possible to use lower-cost ATE systems than those used for cluster functional testing. However, you can implement cluster-functional test's divide-and-conquer strategy *and* conform to the testability bus standard at the same time.

An intangible advantage of a testability-bus standard is that it can convert an arm-waving exercise into something quantifiable. In the absence of a standard, determining the difficulty of testing a proposed design can be an exercise in circumlocution. With a standard in place, you can replace hours of fruitless, time-consuming discussions with a simple statement of whether a product does or does not comply with the standard, and if it complies, what level of the standard it meets.

to perform the actual board replacement.

At the nuts-and-bolts level, a seemingly trivial problem—incompatibility among some logic-simulator database formats and the input requirements of some ATPG programs—has placed roadblocks in the way of automatic test-vector generation. The quick solution is database-translation programs. With a little more effort, vendors can modify the simulators and ATPG programs to cure the incompatibilities. For example, they can make their software support relatively new industry standards such as EDIF (Electronic Design Interchange Format).

Another form of incompatibility can also cause problems: ATE systems can't always run the test vectors generated by ATPG software. Some vendors are addressing this problem with software that compares generated vectors against a target tester's resources and flags incompatibilities. You can also use such software to modify the vectors until they are compatible with the tester.

Other vendors are adamant that you shouldn't start designing a product until you fully understand the resources of the ATE system that you will use to test it. At least in US companies, it is very unusual for designers to let tester capabilities constrain their designs, although the idea of doing so is totally consistent with DFT. However, it is quite clear that you will wind up with a usable vector set a lot sooner if you consider the tester's capabilities *before* freezing your hardware design rather than waiting until afterward.

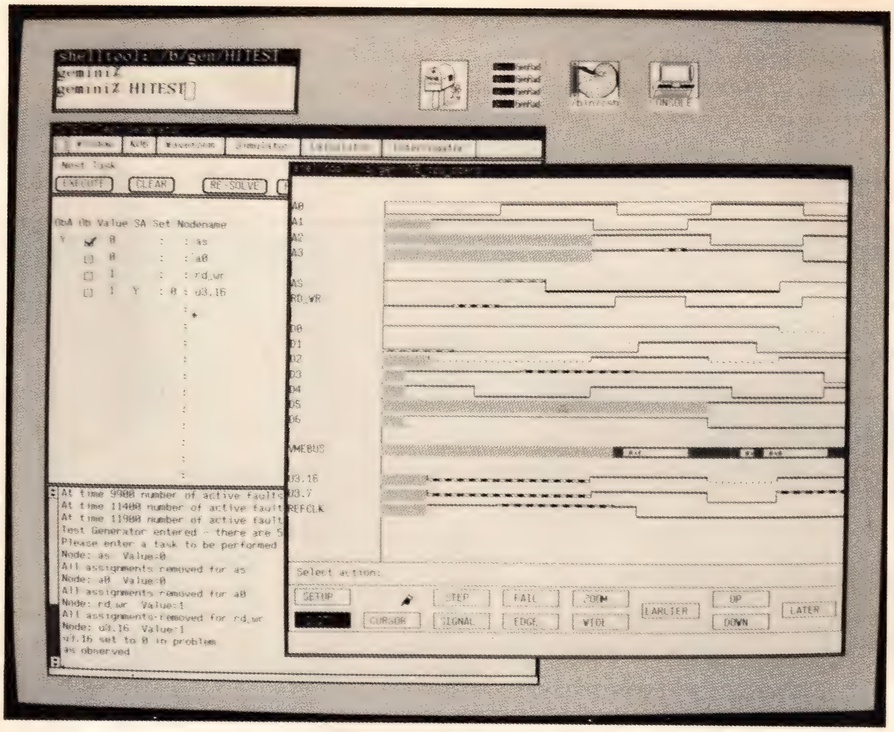
Scannable components needed

A real problem with acceptance of ATPG for board-level designs relates to component availability: To effectively implement the scannable designs required for compatibility with ATPG programs, you need scannable devices. Otherwise, you must create their equivalent from unwieldy numbers of SSI devices. Many ASICs now incorporate circuits that implement at least a boundary-scan approach. Scannable equivalents of the most-used MSI devices and μPs still aren't widely available. (One vendor is represented in **Table 1**.)

Advocates of DFT categorize several of the above concerns as results of a one-sided view of the product-development process. A good example is the fear of lengthened product-development cycles. Today, the test-development phase of a complex-board project often consumes as much time and money as the traditional design phase. DFT advocates insist that once designers are familiar with the new discipline, the cost and duration of the design portion of a project that uses DFT will probably not exceed what you experience using traditional approaches, but the cost and duration of test development can *decrease* by 90% or more. Even if adopting DFT does increase the cost and duration of the design phase by 20%, a 90% decrease in test-development time and cost will cut the overall project cost and duration by 35%. In fact, ATPG vendors cite reduced time to market as the selling point that strikes a responsive chord with more potential customers than any other.

Surprisingly, aside from defense-electronics manufacturers required to comply with MIL testability standards, the few US companies that have adopted DFT for board- and system-level designs have done so in response to pressure not from manufacturing but from strong field-service profit centers. These companies have found that to service their products profitably, they must diagnose and repair board faults at depots located close to their customers. Such depots don't process the volumes of boards that would justify purchases of million-dollar testers. Repair depots need low-cost testers that they can quickly reconfigure to troubleshoot and test boards of many types. Unless the boards are designed for test, low-cost testers won't do the job.

In the Pacific rim, the situation is



```
shelltool: /b/gen/HITEST
geminiZ
geminiZ HITEST
```

```
ObA Ob Value SA Set Nodename
 Y  ✓   0       :   : as
    ☐   0       :   : a0
    ☐   1       :   : rd_wr
    ☐   1   Y   : 0 : u3.16
```

```
At time 9900 number of active faults
At time 11400 number of active fault
At time 11900 number of active fault
Test Generator entered - there are 5
Please enter a task to be performed
Node: as  Value:0
All assignments removed for as
Node: a0  Value:0
All assignments removed for a0
Node: rd_wr  Value:1
All assignments removed for rd_wr
Node: u3.16  Value:1
u3.16 set to 0 in problem
as observed
```

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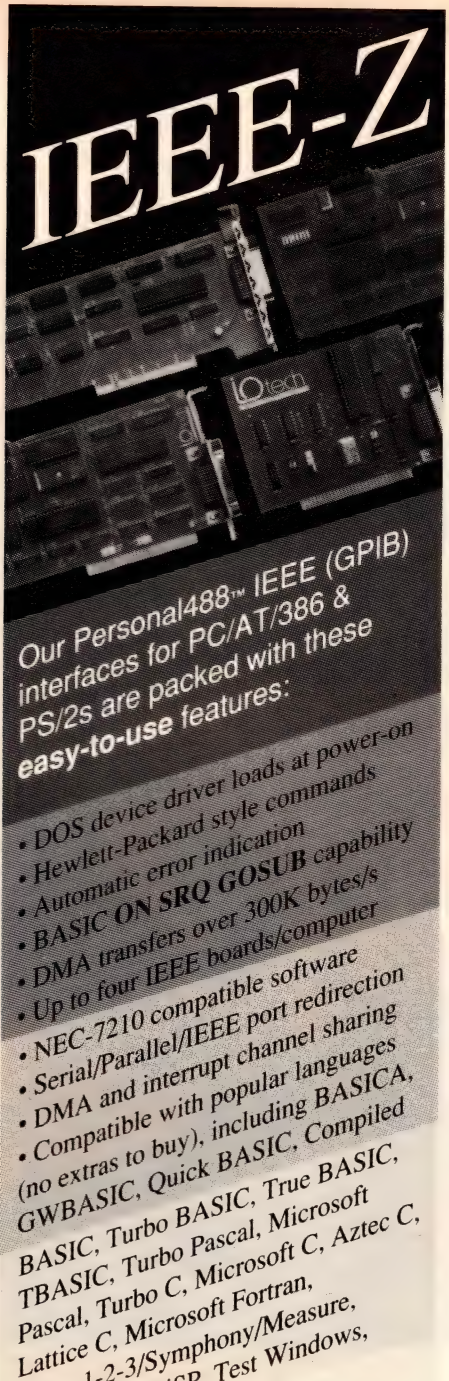

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For more information . . .

For more information on the testability products listed in **Table 1,** circle the appropriate numbers on the Information Retrieval Service card, contact the following manufacturers directly, or use EDN's Express Request service.

Aida Corp
5155 Old Ironsides Dr
Santa Clara, CA 95054
(408) 980-5200
Circle No 701

Anvil Software
Box 901
Arlington, MA 02174
(617) 641-3861
Circle No 702

Gateway Design Automation Corp
6 Lyberty Way
Westford, MA 01886
(617) 692-9400
Circle No 703

Genrad Inc
300 Baker Ave
Concord, MA 01742
(617) 369-4400
Circle No 704

Hewlett-Packard Co
1820 Embarcadero Rd
Palo Alto, CA 94303
Phone local office
Circle No 705

HHB Systems Inc
100 Wyckoff Ave
Mahwah, NJ 07403
(201) 848-8000
Circle No 706

Logical Solutions Technology Inc
310 W Hamilton Ave, Suite 101
Campbell, CA 95008
(408) 374-3650
TLX 172867
Circle No 707

NCR Corp
2001 Danfield Ct
Ft Collins, CO 80525
(303) 226-9500
Circle No 708

Silicon Compiler Systems Inc
2045 Hamilton Ave
San Jose, CA 95125
(408) 371-2900
Circle No 709

Teradyne Inc
321 Harrison Ave
Boston, MA 02118
(617) 482-2700
Circle No 710

Test Systems Strategies Inc
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Beaverton, OR 97005
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TLX 992633
Circle No 711

different. Possibly because of their emphasis on serving geographically far-flung export markets, major Japanese equipment manufacturers, unable to purchase what they consider to be suitable ATPG software, have developed it in house. They are also moving aggressively to design their board-level products so that ATPG software can generate the necessary vector sets.

In the US, the prevalent view is that Asian companies lag behind their American counterparts in software-development expertise. ATPG software is complex; the Japanese companies' ability to develop it in house may indicate that Japanese software development is more advanced than Americans suspect. The Asian companies' decision to focus on ATPG appears to indicate a greater commitment to testability in Japan than in the US, and it provides strong evidence that Japanese hardware designers think of test as *their* problem, not as somebody else's.

If you think about the earlier discussion of the effect of using DFT on a product's availability for use, and if you realize that Asian companies are leading the world in adopting DFT, you come up with yet another reason why American manufacturers should heed the advice of companies urging use of DFT. The push for quality in the US within the past year or two has probably equalized the MTBF of electronic products of similar complexity made in the US and Asia. However, if the use of DFT gives the Asian products a clear edge in availability, US companies will again be uncompetitive.

EDN

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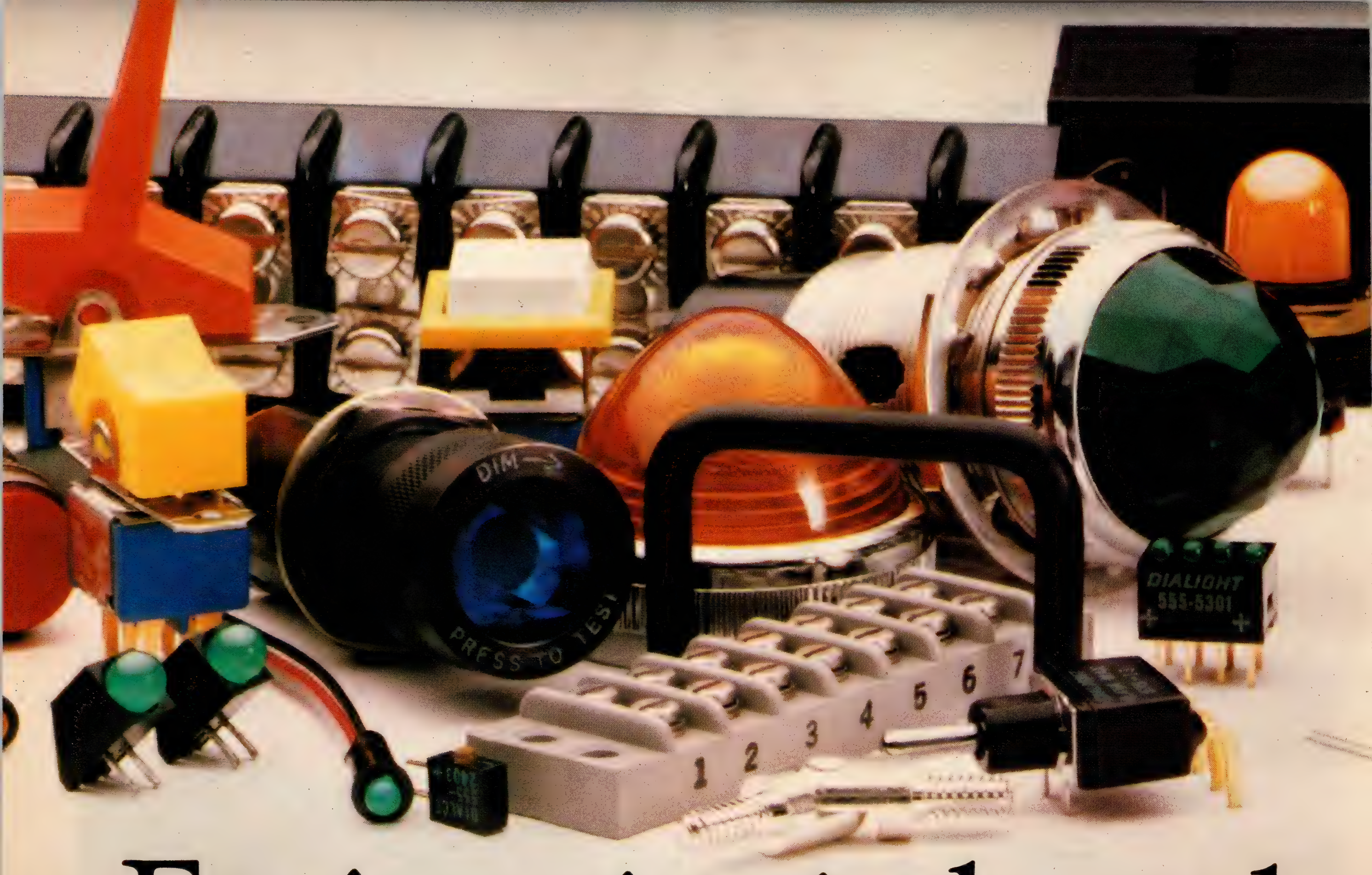

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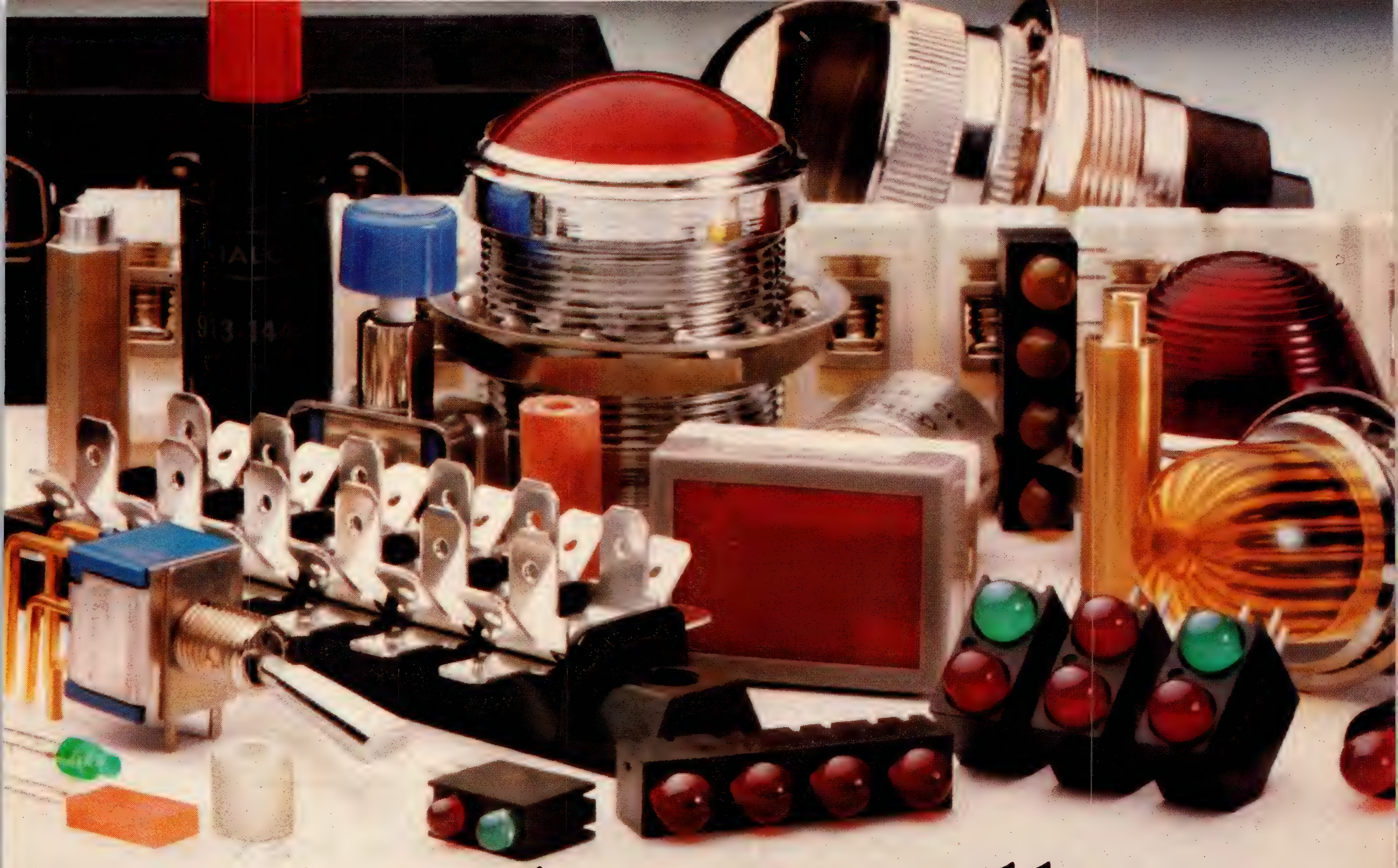

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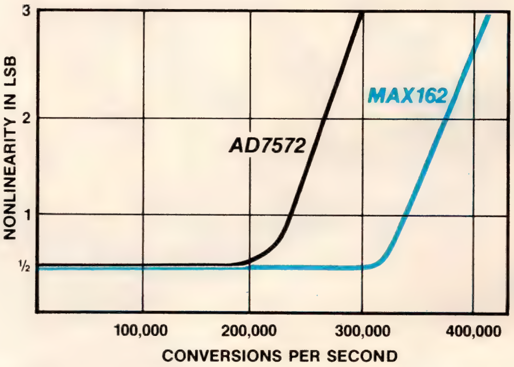

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CIRCLE NO 47

Customer training and reverse engineering promise to escalate the acceptance of CASE

Chris Terry, *Associate Editor*

CASE (computer-aided software engineering) is only now reaching the stage of maturity that CAE tools were at several years ago, but it won't be long before CASE catches up to CAE. As computer hardware falls in price and increases in graphics power, any software engineer who has a PC/AT can make use of CASE tools. More to the point, many CASE vendors have switched the focus of their customer-training courses from promoting specific methodologies to teaching management what they realistically can—and can't—expect from the tools. And finally, new tools have made reverse engineering possible: Reconstructing design diagrams from the source code of existing programs makes program maintenance and enhancement much easier.

CASE isn't a cure-all

Tools for the analysis of software requirements and for the design of software modules have been around since the mid-70s. IBM's HIPO (hierarchical input-process-output) diagrams, Edward Yourdon and Tom DeMarco's data-flow diagrams, Jean Warnier and Kenneth Orr's stepwise-decomposition diagrams, Nassi and Shneiderman's decision diagrams, and others have all proven useful. More recently, Chen and Merise entity-relationship diagrams have facilitated database design.

Although none of these CASE originators ever claimed that their techniques were a panacea for all design problems, CASE has suffered from this misconception. Some of the more vociferous apologists for CASE espoused one or another technique so vehemently and so exclusively that skeptics perceived that adopting a particular CASE methodology for a large project was almost as total a commitment as embracing a new religion. This attitude, and the resistance it engendered, has done much to slow the acceptance of CASE tools.

Moreover, until the advent of inexpensive workstations with good graphics, the cost of using such tools was high. A relatively simple change in functional requirements could require the manual updating of many pen-and-ink diagrams. For this reason, too, conservative analysts and management resisted the introduction of such tools, dismissing them as "arc-and-bubble games."

It was also common knowledge that CASE tools were useful only for new software systems. Nobody in his right mind would ever undertake the labor of constructing design diagrams from the source code of programs that had been running satisfactorily for months or years, but which needed some updating.

CASE-tool vendors readily admit that no one methodology is ideal for all types of software systems, and they are trying to provide a practical education for their customers. Peter Craig, president of Promod Inc, emphasizes that there is still a shortage of software developers trained in the techniques needed for the successful development of large systems. His company's 1-day, in-house seminars focus a customer's attention on the need for new tools, and stimulate serious consideration of which tools and techniques will best meet the needs of the customer's current and future projects.

Craig finds that management is most receptive in companies that are developing embedded systems, and whose engineers have already found that CAE tools have far outstripped the original expectations of their value. Such companies appreciate the potential of CASE tools far more readily than companies that are concerned principally with management information systems.

> Peter Craig of Promod finds the best reception at companies where engineers have already found that CAE tools have far outstripped the original expectations of their value.

John Romano, a product manager at Hewlett-Packard, has also found that customer training is most effective when it avoids a particular methodology initially, and instead concentrates on what management

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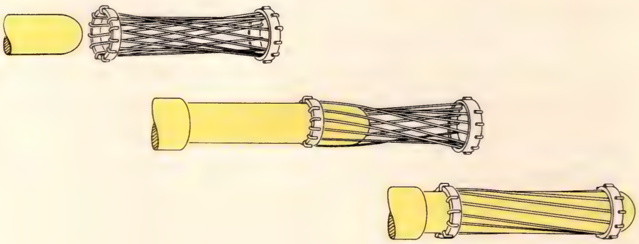

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can and cannot expect from the introduction and use of CASE tools. Romano believes that CASE is still in an early stage of its development, and that all projects that use CASE tools are basically pilot projects. According to him, it's important not to lock users into one particular methodology but rather to discover what they are trying to do, which current tools will best help them to do it, and how best to make data models accessible to all phases of the development process.

Romano also points out that this type of customer training relieves some kinds of pressure from developers, because it convinces management that the use of appropriate CASE tools will yield better quality in the end product. CASE probably won't shorten the total development time, but developers will be able to make better, more effective use of their time.

A less obvious benefit, which can form an important part of a company's return on investment, is that the higher quality of a first deliverable item means less time and energy spent later on maintenance: There'll be fewer defects to correct, and enhancements will be easier to incorporate.

Dave West, president of Visual Software Inc, feels that the key to CASE's wide acceptance is making the tools adaptable to different needs. It's particularly important to extend the tools to cover all phases of development from requirements analysis through coding to maintenance.

Along the same lines, Eyal Levy of Ready Systems Inc expresses the view that CASE will undergo "onionization." The tools available today are just the core of the onion —acceptable, but needing many additional layers to be completely satisfactory. Levy doesn't believe that there will be any total, generalized solution for all problems; rather, new tools and techniques will evolve to provide complete solutions for specific environments such as embedded systems, real-time systems, and databases. Because the needs of each environment are so different, engineers will need a different toolset for each and communication capability between toolsets.

He, too, has found that customer management is confused (and skeptical) about the value of CASE, which is why Ready Systems (which specializes in real-time systems) chose to classify its toolset as CARD (computer-aided real-time design) instead of CASE.

Integration is the challenge

One of the major concerns of CASE-tool users and vendors alike is the need to make CASE-generated design data available during as many phases of a software project as possible. Ideally, this data should also be available in a form that CAE tools and CASE tools from other vendors can also use.

The vendors have achieved the first goal. Requirements-analysis tools generate detailed specifications of data items and processes. These specifications reside in the data dictionary and are the raw material on which the completeness and consistency checks in all phases are based.

> John Romano of Hewlett-Packard believes that CASE is still in an early stage of its development, and that all projects that use CASE are basically pilot projects.

In multiuser workstation systems, the specifications are automatically available to all members of the design team. In a system running on IBM PCs (or compatibles), the obvious course is to link the PCs in a network and let the data dictionary reside on the network file server; in this way, all team members can use and update the data dictionary and drawing files with no delay or conflicts.

Hewlett-Packard's Romano says that the biggest challenge involves linking CASE tools and other development tools. Links currently exist between HP/Teamwork and the company's AX-LS cross compilers, and Romano says that HP's long-term goal is to provide links between HP/Teamwork and all of the company's cross-development tools.

One new tool that uses data generated by HP/Teamwork tools is the AX-BA branch analyzer, which exercises part or all of the C code that the design team generates. You can generate test cases and run AX-BA at any stage of the design; AX-BA then reports all branches that are executed, as well as sections of code that are not executed during the run.

Software-testing considerations affect all phases of your design, and you should certainly take them into account during the requirements-analysis phase. If you start thinking about testing early enough, you can use information residing in the data dictionary as the basis for constructing test cases. At present you may have to export this data to other tools (such as H-P's AX-BA) that actually perform the tests, but vendors are looking to develop and integrate tools that will automatically access the data dictionary, extract the information necessary for generating test data, and then run the tests.

CASE tools, to be fully effective, must facilitate three kinds of communication. All members of a design team must be able to communicate among themselves; tools from the same vendor must be capable of exchanging information; and tools from different vendors must be able to communicate.

A multiuser host or a network of workstations running an integrated set of CASE tools provides the primary communication between team members, who then all have access to the same database. The CASE tools check the work for consistency and completeness according to the same set of rules.

HP's Romano points out that when you're designing a real-time or embedded system, another level of communication is also essential: making sure that the hardware engineers are fully integrated with the design team right from the start of the requirements-analysis phase.

Failure to arrive at a joint hardware/software approach to a design can bring about a situation in which the hardware operates correctly, but requires undesirable or time-consuming software operations, or in which real-time software considerations require modifications to hardware that's already in the manufacturing stage. Such conflicts can be expensive to resolve, and need never arise if the two groups are in continuous communication.

The value of communication between all of a vendor's CASE tools hardly needs any further emphasis. CASE's use of a common data dictionary containing specifications of all data items and processes is what makes possible not only consistency and completeness checking through all of the design stages, but also some of the reverse-engineering techniques that are starting to allow CASE to maintain existing software.

The need for communication between tools from different vendors arises when portions of a very large system are distributed between several subcontractors. (MIL-spec projects are a good example.) Each subcontractor may use a different vendor's CASE tools, but at some point in the project their results have to be combined.

The CAE industry faced this same obstacle several years ago. Several formats existed for interchanges between some specific CAE products, but a growing need for a wider interchange of data resulted in the development of a standard interchange format, EDIF (Electronic Data Interchange Format).

In 1987, Cadre Technologies Inc, one of the leading CASE-tool vendors, proposed extensions to the EDIF format that would permit the exchange of data between CASE tools from different vendors (**Ref 1**). These extensions would place particular emphasis on allowing both interactive and batch data exchange, as well as incremental updates to a database. They would also permit data interchanges between CASE and CAE tools.

A number of vendors are supporting the use of these extensions to EDIF, or are at least serving on a committee whose aims are to refine Cadre's original proposals into a generally acceptable standard. The vendors hope that a widely accepted standard will allow data interchange not only among CASE tools and between CASE tools and CAE tools, but also between CASE tools and a wide range of other existing cross-development and documentation tools.

Software-documentation standards such as DoD-STD-2167 have already had an impact on the growth and features of CASE tools. One of the requirements of this standard is that there must be a clear audit trail from the system-requirements specifications to all software modules. The need for this audit trail has stimulated the development of tools that can provide such cross-checking.

Tools are improving

You won't find many automatic code generators yet, and many people still regard those that do exist (such as EPOS-R from SPS Inc) with a certain degree of suspicion. But you will find a number of tools that partially automate, or at least facilitate, the generation and updating of documentation.

Tekcase from Tektronix, for example, includes an Auditor tool that correlates the software modules and their functions with the design requirements and then reports discrepancies and incomplete items. This tool provides a complete audit trail (vital for compliance with DoD-STD-2167) from requirements analysis to software deliverable items.

Even more important, there are now tools (such as Re-Source in the Promod toolset, and Designer in the Tekcase toolset) that will scan the source code of an existing program or system that is written in Ada, Pascal, or C, and will automatically construct module-design and data-

> Eyal Levy of Ready Systems has found that customer management is confused about the value of CASE—the company calls its toolset CARD (computer-aided real-time design) instead of CASE.

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flow diagrams in the notation of your choice. These tools extend the usefulness of CASE to an installed base of software that was previously inaccessible to CASE tools. Clearly, such tools are invaluable when the need arises to update and enhance existing programs, particularly if the designers of these programs have left the company.

Another standard that may provide even more impetus for the use of CASE is MIL-STD-1840A, which requires that by the year 1990 all documentation on projects submitted to the DoD be in machine-readable form. The increasing complexity of such documentation, which may amount to several thousand pages for large projects, makes it vital to have a means of making changes to one document and the ensuing changes to the many other documents that may be affected. Further, it's essential that there be a means of obtaining the latest version of each drawing and specification that the CASE tools generate.

Context Corp offers a documentation management system that can help you fulfill the requirements of MIL-STD-1840A. The system provides distributed processing on a heterogeneous network of all types of computers from mainframes to workstations. Two important features reduce the problem of keeping track of changes.

The "inclusion by reference" feature allows you to keep just one copy of each reusable text module or drawing on the network server. Thus, for example, if you're going to use a drawing in five different documents, you access it at print time, by means of its name. The copy that you access is always up to date. This feature eliminates the need to maintain a separate copy for each document (with all the inherent problems of updating five copies).

The other feature is a link, either to Cadre's Teamwork or to Teledyne-Brown's Tags suite of CASE tools, that allows you to display or print drawings and specifications generated by those CASE tools. Effectively, if you need a CASE drawing or text for your document, the link requests the CASE tool to supply it in printable form as if it were standard output. Therefore, the link does not need any filter (such as conversion to or from EDIF). Context plans to work with other CASE-tool vendors in the near future to create additional links. **EDN**

Reference

1. Hecht, Alan, and Matt Harris, *A CASE standard interchange format: proposed extension to EDIF 2 0 0*, Cadre Technologies Inc, Providence, RI, 1987.

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For more information . . .

For more information on the CASE tools described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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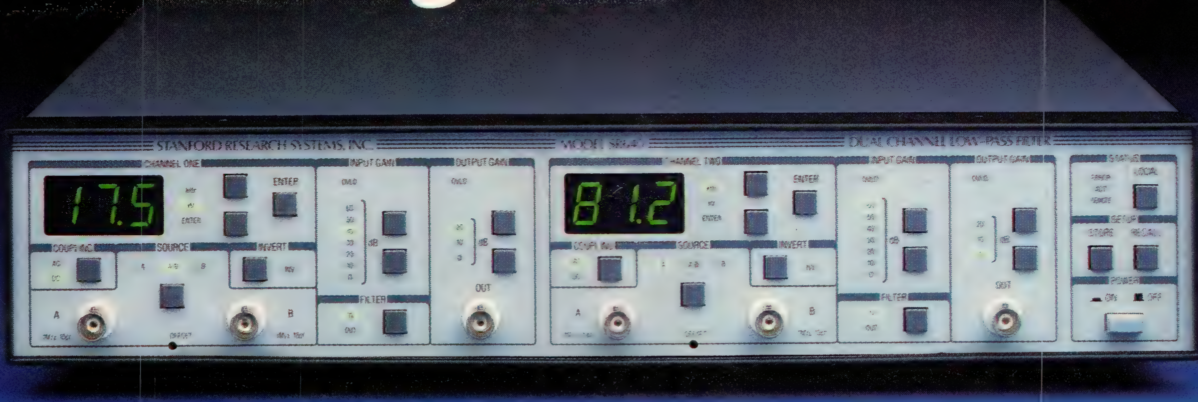

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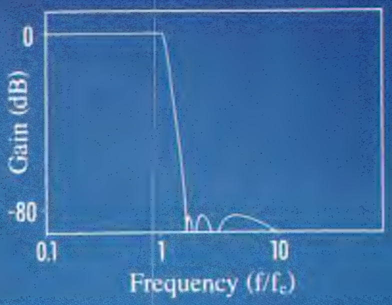

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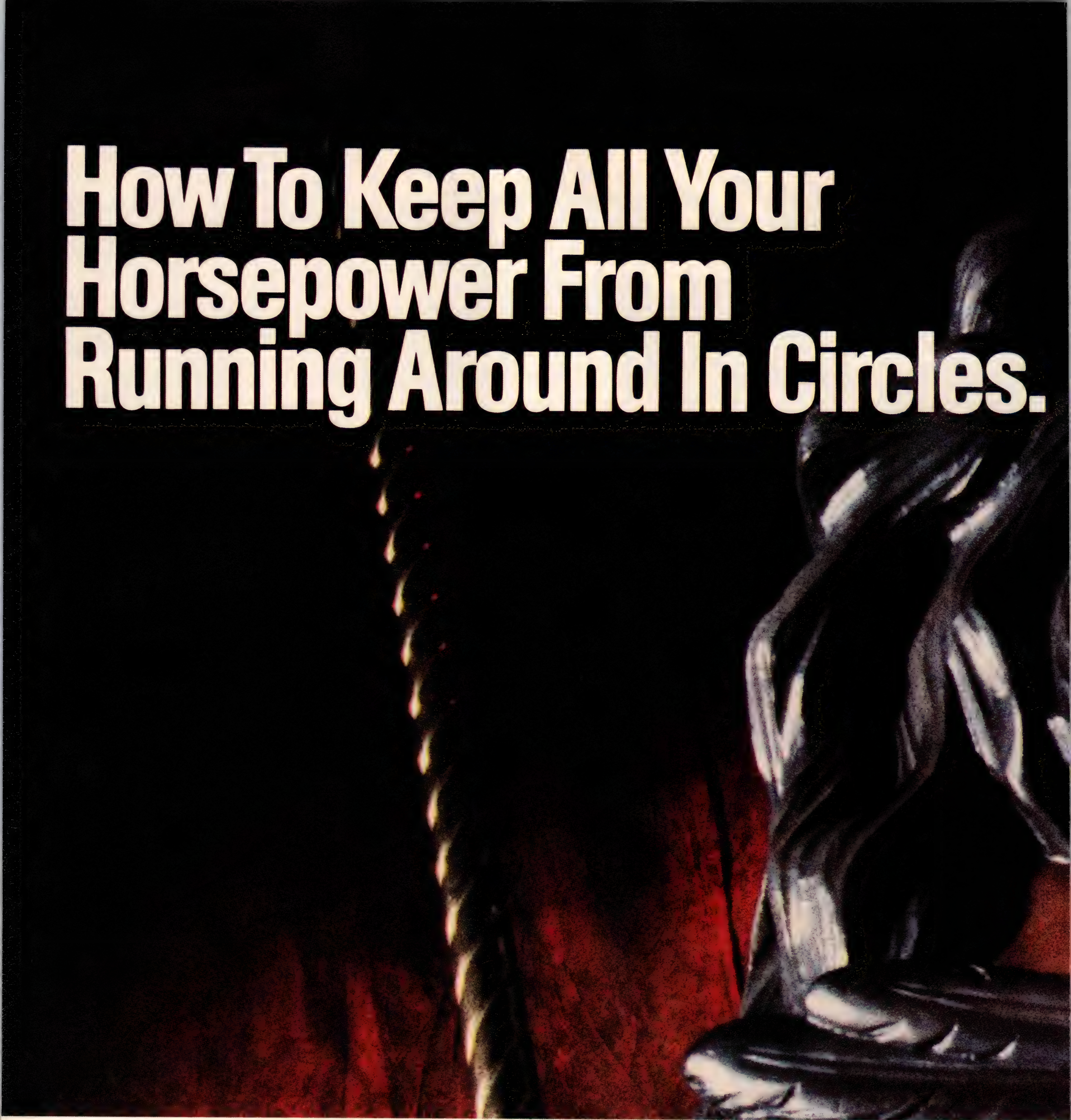

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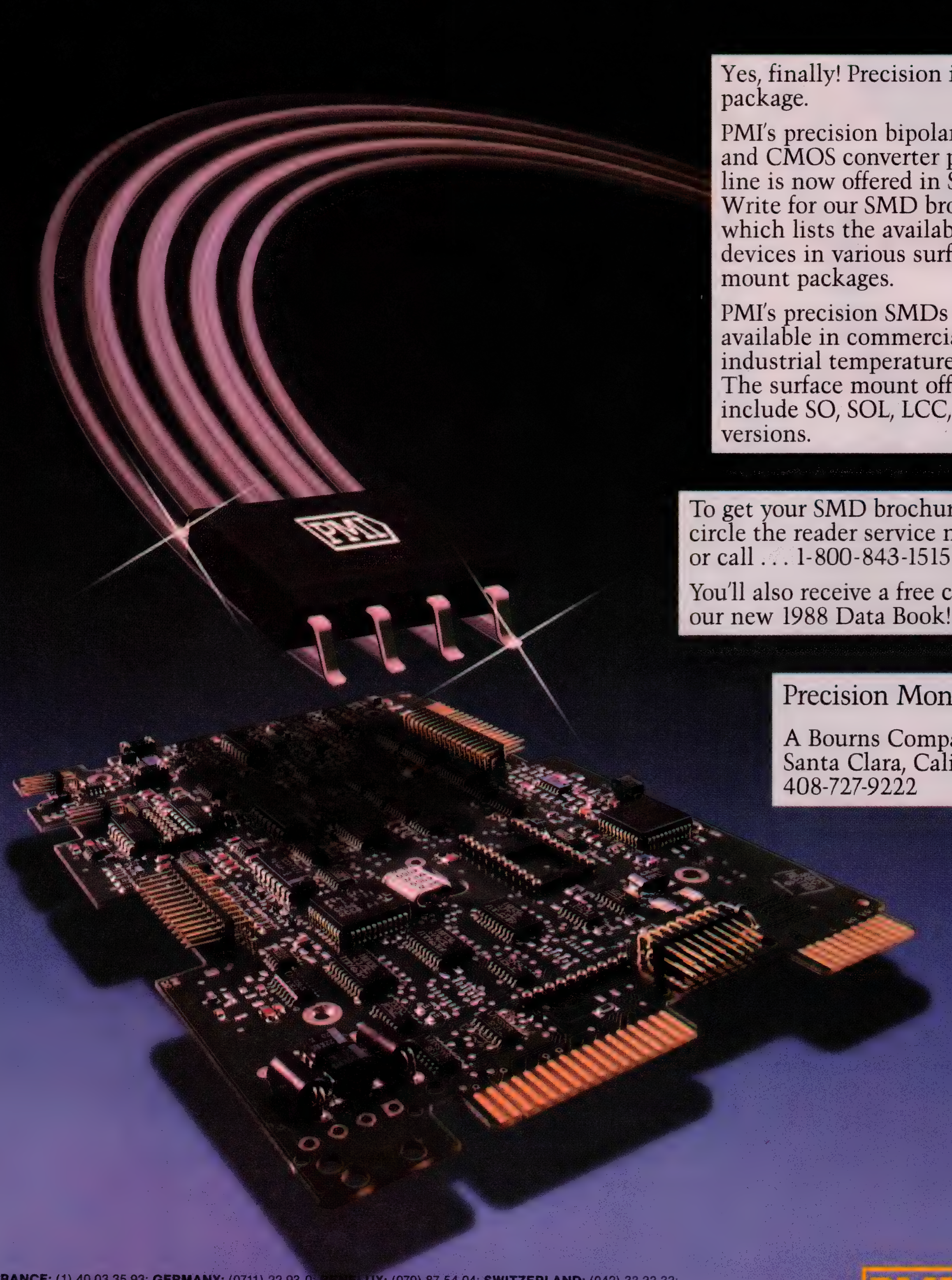

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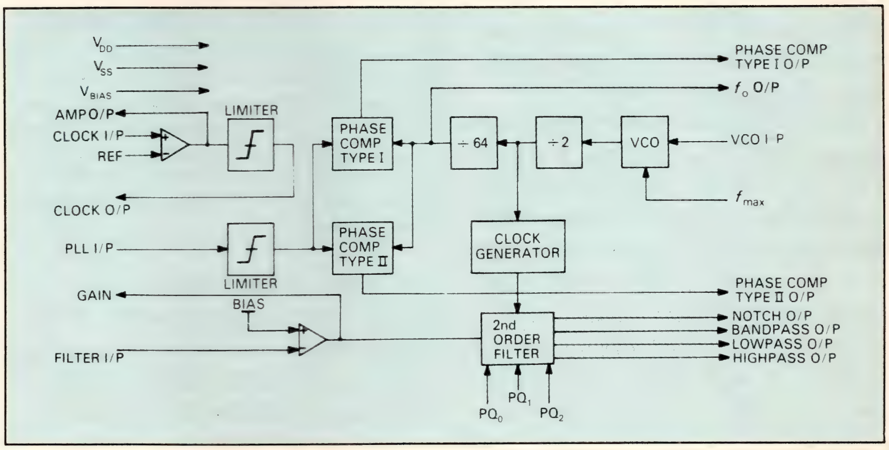
Digitally programmable 1-chip filters yield lower-cost data-acquisition systems

Tarlton Fleming,
Associate Editor

Monolithic filters that combine programmability with the proven advantages of switched-capacitor (SC) technology promise to let engineers develop less-expensive, more versatile data-acquisition systems. By allowing a host processor to control the center frequency (f_0) and quality factor (Q) of an antialias filter, for instance, these devices enable the system to better accommodate a variety of signals within one channel.

Digital programming also enhances the value of SC state-variable (or universal) filters. These filters can produce any of the five basic frequency responses (lowpass, highpass, bandpass, band reject, or allpass), and you can achieve higher values of odd- or even-order response by cascading the filter chips. The state-variable filters are useful for prototyping and for low-quantity requirements. Some of the recent programmable versions let you place the filter's frequency response, f_0, and Q under software control.

Although digital control is a new feature for monolithic-IC filters, companies such as Frequency Devices (Haverhill, MA) have offered digitally programmable conventional (RC) active filters for some time. These products come in 2×4-in. encapsulated modules that cost $150 to $300 each. Monolithic, programmable SC filters, on the other hand, present not only a different array of technical choices, but also smaller size and a lower price ($25 typ). Manufacturers anticipate that these advantages will inspire an increased use of SC filters in programmable applications.



***Based on a phase-locked loop,** this state-variable, switched-capacitor filter from Mx-Com produces a corner (or center) frequency (f_0) that's equal to the PLL reference frequency that you apply to the chip.*

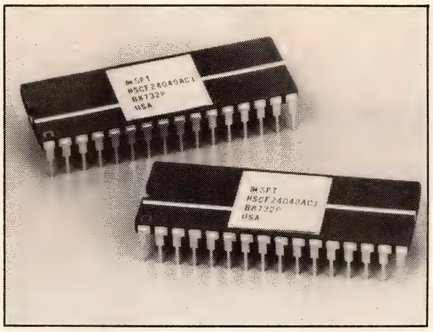
Standard-product filters pose a dilemma for an IC manufacturer's product planners: They must decide whether to offer a universal filter that will be of interest to many customers but only in small quantities, or whether to propose a more efficient design that targets a dedicated application. The second strategy can result in large initial orders, but it entails the risk that a commodity-IC manufacturer may take notice, duplicate the product, and capture much of the business. Competition from ASICs also complicates the planner's job. Manufacturers agree that filters residing on ASICs account for more than half of the new filter applications (aside from the large quantities of committed-purpose filters used in the military and the telecomm industry).

The category of nonuniversal, standard-product SC filters has few members. Exar offers several nonprogrammable devices: The eight XR-1001/1008 Series fourth-order lowpass filters cost $1.30 to $1.55 (100), and the seventh-order, elliptic, lowpass XR-1016 filter costs $5.97 (100).

Honeywell's HSCF24040 is one of the few digitally programmable filters in this category. The monolithic HSCF24040 responds to the widespread need for bandlimiting (antialiasing) protection that precedes the A/D converter in an instrument or a data-acquisition system. The chip's SC section is a seventh-order, Chebyshev, lowpass ladder configuration that emulates a series-inductor/shunt-capacitor, LC-filter network. A 3-bit input code selects one of seven fixed ratios of clock to center frequency (f_{CLK}/f_0). Further, you can vary f_{CLK} as required to obtain any f_0 in the 78-Hz to 20-kHz range.

Filters create alias frequencies

Because the SC filter itself can create alias frequencies as a result of the switched capacitors' sampling action (see **box**, "An overview of switched-capacitor filters"), designers often bandlimit the SC filter by preceding it with a conventional RC active filter. For convenience, Honeywell has included such a 3-pole, continuous-time, lowpass RC filter in the HSCF24040 chip. Internal switches can connect the RC filter either to the SC-filter input, where it provides the antialias function, or to the SC-filter output, where it removes the SC filter's quantization noise. What's more, the RC-filter's f_0 is also programmable—the chip's thin-film resistor network, along with a second 3-bit input code, allows you to select one of eight bandedges over a 12 to 1 range.



Suitable for antialiasing applications, *these seventh-order, lowpass-Chebyshev SC filters from Honeywell offer programmable f_0, dc gain, and output sample rate. The chip includes an RC input filter, also with programmable bandedge.*

The HSCF24040's differential signal path helps to provide a 0.05% THD, a −50-dB PSRR, and an 85-dB (min) dynamic range. This differential path converts to a single-ended path in the output stage (called the decimator). The decimator also provides two programming bits that let you change the output-sample rate ($f_{S/H}$) to a multiple of 25, 12.5, 6.25, or 4.167 times f_0. (A sample/hold function is inherent in the output stage, and by changing $f_{S/H}$ you can adjust the Hold period to accommodate different A/D-conversion times.) Finally, the last two programming bits let you set the HSCF24040's overall gain to a value of 1, 2, 4, or 8. The device costs $26.90 (100), comes in a 32-pin DIP, operates on ±5V, and dissipates about 150 mW.

One other programmable, non-universal SC filter is the ML202CP telephone-line equalizer from Micro Linear. This CMOS chip compensates for the frequency response of a telephone line by adjusting the signal spectrum's height (gain peak at 3250 Hz), its bandwidth, and the slope of its lower bandedge. You program these parameters by loading the chip's serial-data input with a 14-bit word that contains 4 bits each for the height, slope, and bandwidth. The device contains a clock

An overview of switched-capacitor filters

If you need a frequency-agile, easily adjusted filter, or if ease of manufacture, simplicity, and freedom from calibration are paramount in your filter design, you should consider using a switched-capacitor (SC) type. For such applications, the SC filter's advantages may outweigh the noise, charge-injection, and alias-frequency effects that are inherent in the SC technology.

SC techniques were developed in the 1930s, but the first practical SC filters didn't appear until the 1960s, after the advent of the integrated circuit. AMI (now Gould Inc, Santa Clara, CA) introduced dual-tone multifrequency (DTMF) filters late in that decade, followed by EG&G Reticon and others; National Semiconductor's dual universal filter (the MF10) became an industry-standard component. Those early products suffered performance limitations related to the evolution of CMOS analog switches and op amps: They had low bandwidth; high levels of noise and clock feedthrough; tight power-supply tolerance; and excessive input-offset voltage, which was caused by charge injection from the switches. Today's SC filters offer much-improved specs, however, thanks to the ongoing refinements in circuit design and process technology.

Unlike digital filters, which operate on bit-parallel, digitally encoded data, SC filters and their conventional RC-filter counterparts operate on continuous analog-voltage waveforms. SC and RC filters employ similar feedback networks around op amps, except that the SC circuit substitutes switched capacitors for the RC circuit's resistors. The SC filter's major disadvantage is the switching action that introduces discrete-time sampling in an otherwise continuous signal-processing circuit. Like an A/D converter, the SC filter produces phantom (alias) frequencies when operating on signals that exceed ½ the sampling (switching) frequency.

When alias frequencies are a problem, you must add a continuous-time bandlimiting filter at the SC filter's input. That is, you must provide an RC filter as antialiasing protection for the SC filter, which often is being used as antialiasing protection for something else! Adding the RC filter is justified, though, by the SC filter's advantages: The SC filter has few external components and an easily variable center frequency (f_0), and its precise operation is stable both over temperature and from unit to unit. A high switching rate (f_{CLK}) within the SC filter will ease the RC filter's job and generally minimize your concerns about aliasing.

SC filters usually fix the internal f_{CLK}/f_0 ratio at 50 or 100; you then change f_0 by varying f_{CLK}. In these applications, the RC antialiasing filter (if one is present) must maintain its f_0 at a respectful distance from the SC filter's f_0. This requirement has led to an emerging need for RC lowpass filgenerator; a 2-pole antialiasing filter; a highpass SC filter for 60-Hz rejection; height, slope, and bandwidth SC filters; and a 2-pole RC smoothing filter at the output. It costs \$8.95 (100), consumes 6 mW from ±5V supplies, and comes in a 16-pin DIP.

A filter for all seasons

The universal filter's versatility has made it attractive to many filter manufacturers. Among the SC-filter offerings that are not digitally programmable, Linear Technology Corp's dual-filter LTC1060CN and triple-filter LTC1061CN are notable for their low levels of output noise: That parameter remains well under 100 μV rms in many configurations, exclusive of clock feedthrough. The LTC1060CN costs \$3.90 (100); the LTC1061CN sells for \$8.25 (100). (LTC also plans to introduce a monolithic quad filter later this year that features noise levels approximately half those of the LTC1061.) Micro Linear's dual universal ML2111CCS, which costs \$7.15 (100), has the distinction of the highest available f_0 (150 kHz, with Q as high as 20).

Among universal SC filters with digitally programmed functions, the MX406P from Mx-Com provides a 3-bit input for setting eight values of Q between 0.54 and 8.0. The usual parallel outputs (lowpass, highpass, bandpass, and notch) are available, and you can set f_0 between 100 Hz and 5 kHz. The CMOS chip includes a phase-locked loop (PLL), which generates the internal clock signal at a frequency that is 64 times f_0; you supply the PLL with a reference frequency equal to the desired f_0. This part costs \$5.63 (100), comes in a 22-pin DIP, operates on 5V, and consumes about 15 mW.

EG&G Reticon's RU5620A provides higher-resolution programming of Q and f_0. One 5-bit word lets you vary the f_{CLK}/f_0 ratio from 50 to 200 in 32 logarithmic increments; you can set f_{CLK} as high as 1.25 MHz. A second 5-bit word sets Q to one of 32 values between 0.57 and 85.0, again in logarithmic increments. The NMOS chip costs \$4.70 (100), comes in an 18-pin DIP, operates with bipolar supplies in the ±5 to ±10V range, and consumes 200 mW max (quiescent) at ±10V.

---

ters with digitally programmable corner frequencies.

The SC filter's output (a staircase of quasi-dc voltage levels) resembles that of a D/A converter. You can remove this quantization noise, if necessary, by adding another simple RC filter such as a passive RC network. But if the SC filter drives an A/D converter, the staircase output represents a sample/hold function that's potentially useful as an interface to an A/D converter. You must synchronize the converter with the filter, and the Hold interval must exceed the conversion time. Honeywell's HSCF24040 filter, for example, lets you change this Hold time by altering the output sample rate independently of f_{CLK}.

What's a biquad?

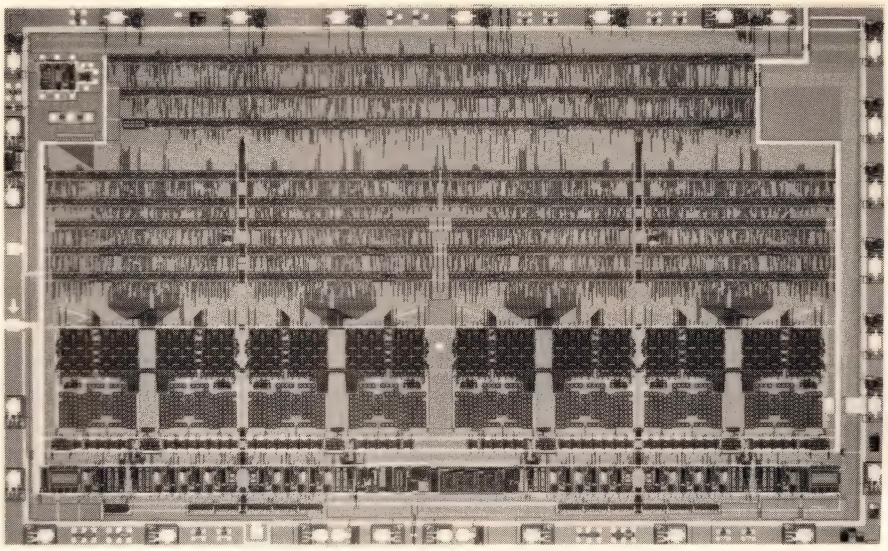
The majority of SC-filter products comprise one or more second-order sections whose transfer function, H(s), has the form

$$H(s) = \frac{As^2 + Bs + C}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2},$$

where s is the complex-frequency variable and $\omega_0 = 2\pi f_0$. In the general case shown in the equation, the numerator and the denominator are quadradic (second-order) expressions, and there are two of them, so the function is labeled "biquadratic" or "biquad" for short.

Many circuit topologies yield (realize) the biquad transfer function, but the state-variable realization lets you set selected numerator coefficients to zero. The resulting "universal" circuit can give you a lowpass filter ($A=B=0$), a highpass filter ($B=C=0$), a bandpass filter ($A=C=0$), or a band-reject filter ($B=0$). Using all three coefficients gives you the allpass (phase-shift) filter. (Note that some engineers refer to the universal state-variable filter as a biquad, but others reserve the term "biquad" for a particular second-order bandpass filter that maintains constant bandwidth as you vary f_0.)

Finally, four attributes define any filter: the type (lowpass or highpass, for example), the f_0 (which is called "center frequency" in bandpass and notch filters, and "corner frequency" in lowpass and highpass filters), the passband gain, and the Q. As the "quality factor" for second-order functions, Q serves as a figure of merit for the filters corresponding to those functions. For bandpass and notch filters, Q measures the sharpness of the response: $Q=f_0/(f_H-f_L)$, where f_H and f_L are the filter's upper and lower −3-dB frequencies. For lowpass and highpass filters, Q describes the degree of amplitude peaking in the vicinity of f_0. By bringing one or more of these four attributes under software control, digitally programmable SC filters are expanding the capabilities of electronic systems.



Containing four universal filter sections, *this SC filter from Crystal Semiconductor offers digitally programmable f_0, filter order, and operating mode. The CMOS chip also includes a user-configurable input op amp and another uncommitted op amp.*

You can achieve even higher resolution and more comprehensive programming of SC-filter functions by choosing a programmable device such as those from Crystal Semiconductor or Maxim Integrated Products. First, Maxim's MAX260/261/262 series of dual, second-order, universal filters gives you separate control of f_0 and Q for each of the two independent sections. An internal memory stores the configuration data: Two 2-bit codes set each filter section in one of four modes, two 7-bit codes set each Q to one of 128 values (0.500 to 64.0 or 0.707 to 90.5, depending on the mode), and two 6-bit codes set each f_{CLK}/f_0 ratio to one of 32 values. (You can obtain any intermediate ratio, of course, by varying f_{CLK}.)

Model MAX260BCNG has the highest range of f_{CLK}/f_0 values, giving it the lowest f_0 (7.5 kHz max) and the best spec for input-offset voltage (250 mV max). This device also includes autozero circuitry that improves the low-frequency performance while providing a sample/hold function at the chip's notch/highpass/allpass outputs. Its price is $7 (100). Models MAX261 and -262, on the other hand, each contain an uncommitted amplifier that you can use for input anti-aliasing or output smoothing. Model MAX261BCNG has a maximum f_0 of 30 kHz (with a Q of 8) and costs $8.50 (100). Model MAX262BCNG achieves a maximum f_0 of 75 kHz (with a Q of 8) by employing a lower range of f_{CLK}/f_0 ratios; it costs $11 (100).

All three models operate on 5V or ±5V supplies and come in 24-pin DIPs. Because the pinout allows only two data pins and a 4-bit address, you must program the chip by writing a 16-word sequence of 2-bit words. Maxim offers four filter-design programs to simplify this task; the programs are free to customers who purchase any of the three filter models. When you use the programs, you first express the desired filter response in frequency-domain terms (f_0, Q, passband ripple, and stopband attenuation). The programs calculate the necessary poles, zeros, Qs, and filter stages,

For more information . . .

For more information on the digitally programmable, monolithic filters discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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Circle No 725

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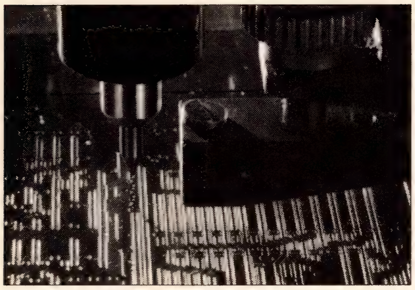

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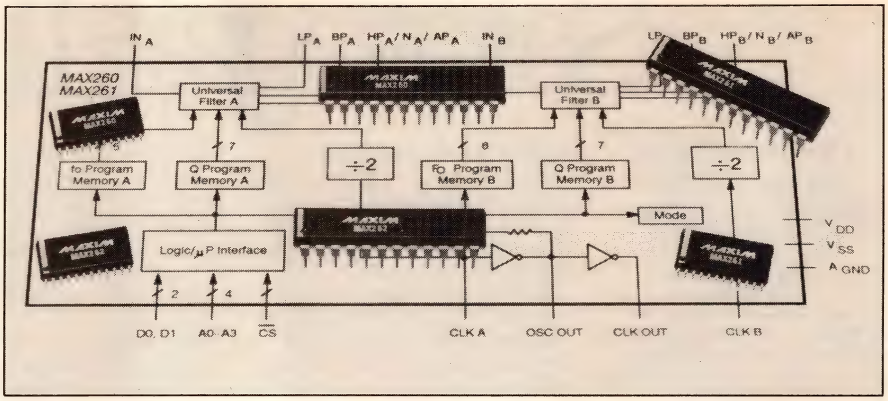

Dual universal SC filters *from Maxim's MAX260 Series let you program the filter's f_0 and Q, as well as its operating mode.*

and compute the required digital input codes. You can load these codes into the chip via the parallel port of a personal computer, using a short Basic program listed in the filter's data sheet.

Four biquads in a single chip

Crystal Semiconductor's monolithic, CMOS CS7008 is a more elaborate filter that contains four universal "biquad" SC sections. Available in a 28-pin DIP, the device has six data lines and six address lines, which give you access to a 6-bit×64-word memory for storing the configuration data. An 11-bit word configures the biquads in a cascade of 1, 2, 3, or 4 sections, and a 3-bit clock-divide code sets f_0. For each biquad, a 2-bit word sets the filter mode. The remaining memory stores 11-bit words that define each of 24 programmable capacitors (six in each section).

The CS7008 lets you define any second-, fourth-, sixth-, or eighth-order response, including lowpass, highpass, bandpass, allpass, notch, lowpass notch, and highpass notch. Corner frequencies (f_0) can range from 1 Hz to 25 kHz typ (the manufacturer hasn't yet determined the max f_0). The chip includes an op amp that's connected to the input for use as a gain amplifier or RC anti-aliasing filter, and another uncommitted op amp for general use. The company also makes the CS7004, which is pin compatible with the 7008, but contains two biquad sections instead of four.

Before either chip can function, you must load it with valid data. Crystal's CDS7000 development system computes this data for you; the system includes an in-circuit emulator that provides immediate feedback on the proposed filter's performance. The CDS7000 consists of menu-driven software, the emulator-electronics module, and cables. You must provide an IBM PC or compatible computer with an 8087 math coprocessor, a Hercules monochrome graphics card (or a compatible card), 256k bytes of memory, and PC-DOS or MS-DOS version 2.1 or higher. The CS7008-P filter costs $30 (100); Crystal expects this price to drop by a third within nine months. The CDS7000 development system costs $3595. **EDN**

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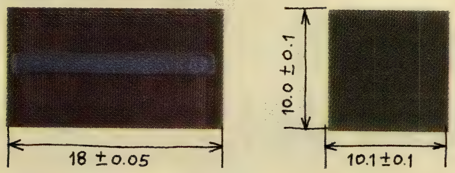
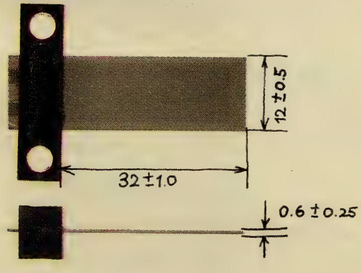


Bimorph type NLB-40 × 12 × 1



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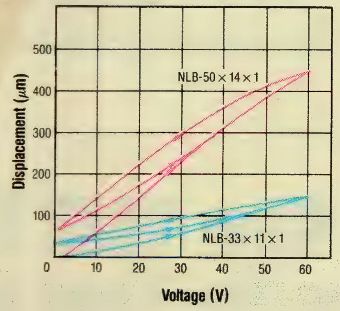
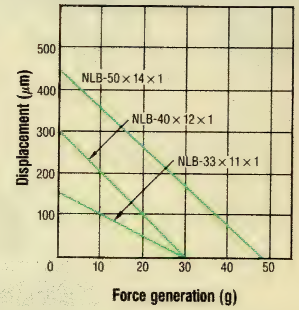
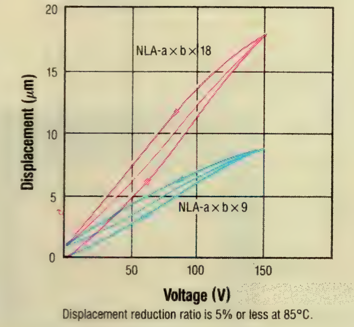
Voltage vs. Displacement



Force generation vs. Displacement (measured at 60V DC)

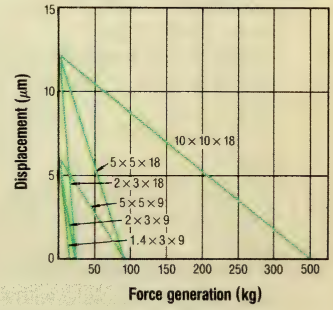


Voltage vs. Displacement



Displacement reduction ratio is 5% or less at 85°C.

Force generation vs. Displacement (measured at 100V DC)



Performance

	Dielectric displacement	Force generation
Stack type	(μm/100V) ±10%	(kg/100V) ±20%
NLA-1.4 × 3 × 9	6.5	14.0
NLA-2 × 3 × 9	6.5	21.0
NLA-2 × 3 × 18	15.0	21.0
NLA-5 × 5 × 9	6.5	87.0
NLA-5 × 5 × 18	15.0	87.0
NLA-10 × 10 × 18	15.0	350.0
Bimorph types	(μm/60V) ±20%	(g/60V) ±20%
NLB-33 × 11 × 1	150	30
NLB-40 × 12 × 1	300	30
NLB-50 × 14 × 1	450	48

CIRCLE NO 55

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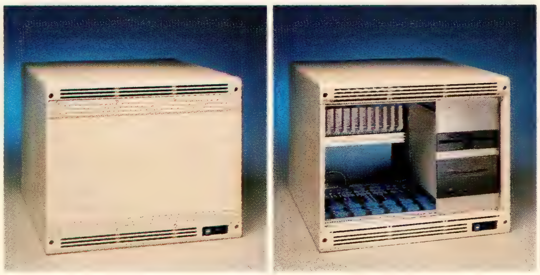

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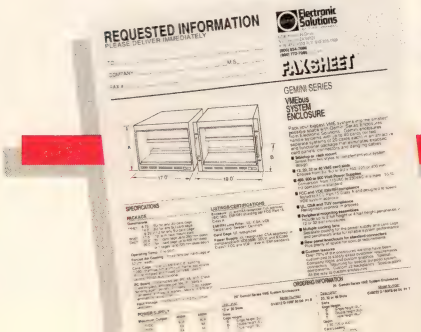

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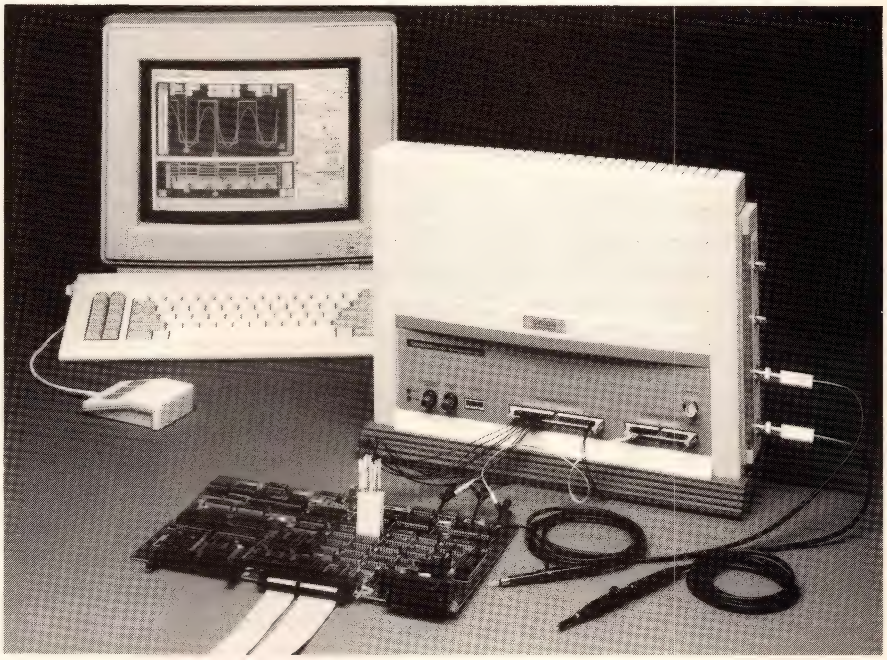


***Performing both digital and analog sampling at 204M samples/sec,** the Omnilab 9240 lets you run DSO and logic-analysis functions simultaneously. You use a host PC/AT or compatible computer for control, display, and data storage.*

The Omnilab 9240 combines a full-function 100-MHz digital storage oscilloscope (DSO) with a 48-channel logic analyzer. The unit is housed in a 15×5.4×11.5-in. enclosure with its own power supplies, and it requires a PC/AT or compatible computer for display and control.

The fact that the instrument executes the functions of both a DSO and a logic analyzer doesn't detract from its performance. Consider the DSO function, for example. The Omnilab 9240 can digitize one channel at 204M samples/sec and two channels at 102M samples/sec. For repetitive waveforms, the DSO has an equivalent-time-sampling rate of 680M samples/sec on both channels. **Table 1** gives some of the key specifications for both the DSO and the logical-analyzer functions.

When you acquire waveforms with the instrument, you can use its signal-averaging mode to reduce noise, or you can choose point-accumulate, envelope, or normal mode. After acquiring a waveform, you can scroll through the entire waveform record or zoom in on a specific area. The standard 4k-sample record memory holds enough data to fill 12 screens. Besides obtaining the standard waveform displays, you can select cursors for digital readouts of voltage or time. You can also choose other digital readouts—such as frequency, rise time, and peak-to-peak voltage—for continuous display. The display is updated 15 times/sec.

When it's used as a logic analyzer, the Omnilab 9240 can sample asynchronously at rates as high as 204M samples/sec. Unlike most logic analyzers, the Omnilab 9240 has equivalent time sampling, a DSO feature that gives you the equivalent of a 680M-sample/sec rate on 48 channels for repetitive events. This feature gives you 1.5-nsec timing resolution for repetitive events. For synchronous clocking applications, you can sample at as much as 34M samples/sec on all 48 channels. The vendor offers disassemblers for more than 100 different microprocessors.

The instrument also lets you use the DSO and logic-analysis functions simultaneously. At 34M samples/sec, you can use two DSO channels and 32 logic-analyzer channels. For repetitive signals, you can use two DSO channels and 32 logic-analyzer channels, all with equivalent

TABLE 1—OMNILAB 9240 SPECIFICATIONS

DIGITAL-STORAGE-OSCILLOSCOPE FUNCTION	
BANDWIDTH	100 MHz
MAX SAMPLE RATE	204M SAMPLES/SEC
RECORD LENGTH	4k SAMPLES (64k SAMPLES OPTIONAL)
VERTICAL RESOLUTION	8 BITS
VERTICAL SCALING	5 mV/DIV TO 10V/DIV
LOGIC-ANALYZER FUNCTION	
ASYNCHRONOUS OPERATION	48 CHANNELS AT 34M SAMPLES/SEC
	16 CHANNELS AT 102M SAMPLES/SEC
	8 CHANNELS AT 204M SAMPLES/SEC
SYNCHRONOUS OPERATION	48 CHANNELS AT 34M SAMPLES/SEC
SETUP TIME	1 nSEC
HOLD TIME	4 nSEC
GLITCH DETECTION	5 nSEC

time sampling at 680M samples/sec. The logic-analyzer and DSO displays are time correlated.

The instrument's triggering functions include the standard analog slope and level triggering for signals within the DSO's 100-MHz bandwidth. Because the Omnilab 9240 is also a logic analyzer, its DSO function can share many trigger functions that are usually found only on logic analyzers.

You can trigger from the digital state of a group of digital-input channels while observing an analog input with the DSO. Because the digital-triggering section uses a high-speed RAM look-up table rather than comparing bits with a trigger register, the trigger can be any set of values in an 8-channel group. You can logically combine multiple 8-channel groups for trigger conditions requiring more than eight channels.

The triggering circuitry also allows you to specify as many as four sequential events combined with event counters that can count as many as 1 million events before triggering. The instrument can also use clock-driven counters to qualify an event by time duration.

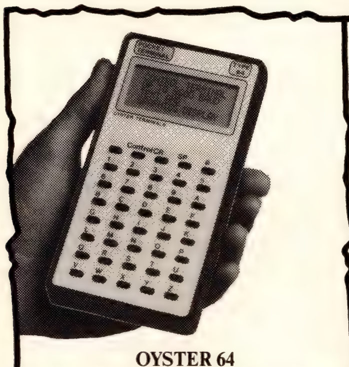
The 8-bit output of the DSO's A/D converters is also routed to high-speed RAM look-up tables. These look-up tables allow you to trigger from a programmed voltage range, and you can use timing qualifiers. For example, you could trigger on a voltage that remains within a specified range for too long a period of time.

In addition to its DSO and logic-analysis functions, the Omnilab 9240 provides 24 digital-stimulus channels with a 4k-bit (or an optional 16k-bit) pattern memory. The stimulus generator, which has a maximum clock rate of 34 MHz, has 3-state outputs that allow you to drive bidirectional signal lines.

The stimulus generator also has an analog-output channel: An 8-bit DAC provides analog stimulus generation over a full-scale amplitude range of 8 mV to 8V. The instrument's standard function-generator outputs include sine, triangle, and square waves, but you can also generate your own waveform or play back waveforms captured by the DSO. The stimulus generator can run simultaneously with the logic analyzer and DSO. The Omnilab 9240 costs $8900.—***Doug Conner***

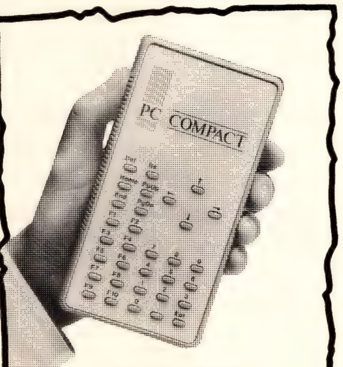
Orion Instruments Inc, 702 Marshall St, Redwood City, CA 94063. Phone (415) 361-8883. TLX 530942.

Circle No 699



OYSTER 64

Graphics LCD for diagrams. special characters, etc., with 16 char. x 4 lines in text mode; redefinable keyboard; 75-9600 baud; range of interfaces.



PC COMPACT

Hand-held replacement for an IBM PC, XT, AT, PS/2 and compatible keyboards. 32 keys on standard keyboard.

OYSTER 84B

20 char. x 4 line LCD, battery-powered, 8K memory, control character display, 75-19200 baud, range of interfaces.

OYSTER RT80

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CIRCLE NO 57

ZILOG

Z280

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Imagine the savings in cost and board size when you have peripherals like 4 DMA channels that'll give you transfers at 6.6 Mbytes/sec, and a full-duplex UART.

	Z280™	80186	68070
Package	68-pin PLCC/CMOS	68-pin LCC/NMOS	84-pin PLCC/CHMOS
Typical Power	375 mW	2 W	800 mW (est)
Speed	10-25 MHz	8-12.5 MHz	10 MHz
Memory Support	16 Mb Physical Paged	1 Mb Physical Segmented	16 Mb Physical 8 or 128 Segments
16-bit Registers	12 General	8 General	15 Dedicated
Instruction Pre-fetch	256-Byte Assoc. Cache; Burst Mode	6-Byte Queue	None
Multiprocessor Support	Local or Global	Local only	Local only
Wait Logic	Programmable	Programmable	Hardwire
DMA	4 Channels, 6.6 Mb/s @ 10 MHz	2 Channels 2 Mb/s @ 8 MHz	2 Channels, 3.2 Mb/s @ 10 MHz
Counter/Timers	3 16-bit	3 16-bit	2 16-bit
Serial I/O	1 Full-Duplex UART	None	1 Full-Duplex UART
DRAM Controller	10-bit Refresh	None	None
Price (100)	$33	$43	$50

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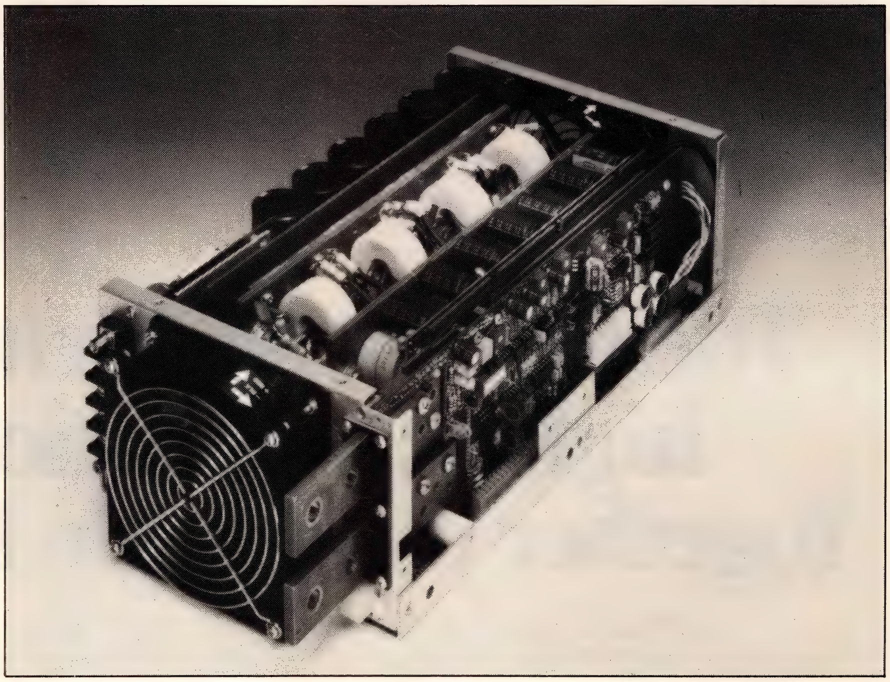
CIRCLE NO 58

Single-output current-mode power supply packs 3000W in a 5×8×13½-in. package



***The four inverters employed in each Series 9R supply make** it fault tolerant and permit it to continue operating even if one of the inverters fails.*

Series 9R power supplies comprise 2, 3, 5, 12, 15, 24, 28, 36, and 48V devices. Each of the current-mode switchers outputs 3000W and fits in a 5×8×13½-in. package—only 4 in. longer than the industry-standard 1500W package.

The 3000W rating derives from the four inverters that operate in parallel within each device. The inverters share equally in the production of output current because they are synchronized and employ current-mode control; the current-mode design also lets you connect multiple power supplies in parallel.

The multiple inverters furnish a degree of fault tolerance to a system in which you use a Series 9R supply. Should one of the device's four inverters fail, the supply will continue to operate at a reduced power level; for example, if only three of a 5V, 600A supply's inverters are operating, it can nonetheless produce 500A.

Consequently, you can specify a 3000W supply in a system that only requires 2500W and thereby ensure that the system will continue to operate even if an inverter fails. If one does, the power supply outputs a TTL signal indicating the condition. The system operator can then replace the power supply at his or her convenience.

Series 9R supplies meet domestic and international safety standards. They operate from a 120 or 208V ac 3-phase source, or from a 230V ac single-phase source. You can power them with a 200 to 365V dc source.

The supplies typically operate at 75% efficiency when running from a 230V ac source. When operating in the 0 to 50°C range, they supply 100% of their rated load, although the 2V device can only supply 1400W because of ouput-bus-bar and rectifier-diode current-carrying limitations.

Current-limiting circuitry in the supplies regulates their maximum peak current to 120% of their rated current, and the devices recover automatically upon removal of the short-circuit or overload condition. In the event of overvoltage, the supplies' inverters shut down at factory-set trip points. For further overvoltage protection, you can specify an SCR-crowbar feature as an option.

The devices have terminals for remote sensing, and you can remotely control the supplies' output to within ±10% of nominal. The supplies also produce signals indicating valid output or input-power failure.

Other key specs include the greater of 5 mV or 0.1% for line regulation, and the greater of 10 mV or 0.2% for load regulation; dynamic response of 4% max output deviation as a result of a 25% step load change; output recovery within 1% of nominal in 200 µsec; and thermal regulation of ±0.02%/°C.

The vendor is shipping samples of the Series 9R supplies. $1800.

—Maury Wright

Bonar Powertec, 20550 Nordhoff St, Chatsworth, CA 91311. Phone (818) 882-0004. TWX 910-494-2092.

Circle No 700

New wings for DSP.

Motorola announces availability of the first real C language compiler for DSP applications.

A new dawn has arrived for DSP programmers. Using the new C language compiler from Motorola you can now write DSP code using a high level language. The DSP56KCC C-compiler is a full Kernighan and Ritchie C implementation supporting development of the high performance DSP56000 family applications.

This easy-to-use program features compiler assembly language with full in-line code capability and a C-lanaguage preprocessor to support MACRO expansion, file inclusion, and conditional compilation. Using it, programmers can peform the entire compilation process in a single step. It also facilitates incremental compilation so that your time-critical DSP codes can be optimized.

The DSP56KCC is available for use on the IBM PC for MS DOS and PC-DOS, Sun 3 for UNIX BSD 4.2, VAX for VMS Version 4.2, VAX for UNIX BSD 4.2, and for the Macintosh II.

The DSP56KCC is available for use on the IBM PC for MS DOS and PC-DOS, Sun 3 for UNIX BSD 4.2, VAX for VMS Version 4.2, VAX for UNIX BSD 4.2, and for the Macintosh II.

For more information.

For more information about using the DSP56KCC C-cross compiler contact your Motorola sales office. For technical literature on Motorola's advanced line of DSP products, please complete and submit the coupon below.

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DSP56KCCx

Software Summary

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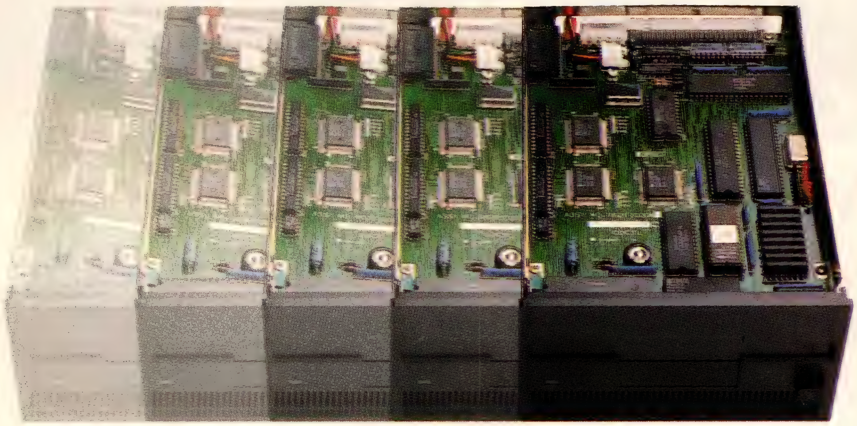

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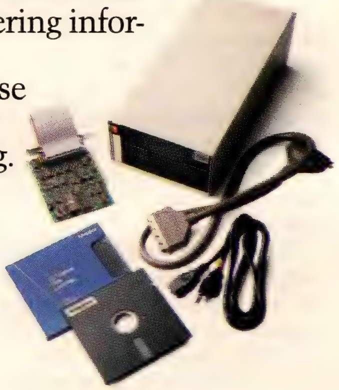

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CIRCLE NO 60

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Maxtor
CIRCLE NO 59

PRODUCT UPDATE

Matrix-switching system connects 2880 cross points

Engineers who work with a lot of relays may be interested in the Model 707 matrix-switching system for electronic-device and -circuit testing. Housed in a 6-slot mainframe that plugs into any IEEE-488 automatic-test equipment (ATE) system, the 707 can connect as many as 2880 cross points on a breadboard prototype of an IC or on a pc board. It also provides a light-pen user interface, which simplifies test development.

You can connect as many as five of the 707 mainframes, each of which can switch configurations of as many as eight 72-pin paths. The cards available for the slots in each mainframe include a general-purpose matrix for microvolt to 200V signal levels, a coaxial matrix for low-noise shielded interconnections, a semiconductor matrix card that automates both current-voltage (IV) and capacitance-voltage (CV) tests through two high-isolation current paths, and a universal adapter card for prototyping or troubleshooting.

Because the unit controls all those switches through one master device, you can set up as many as 200 matrices per second while monopolizing only one IEEE-488 address. The unit's nonvolatile matrix memory retains as many as 100 of those matrix settings for fast-triggered relay sequences or rapid recall. The 707 also provides a simplified wire-connection feature that lets you use standard coaxial cable instead of custom assemblies. In addition, you don't have to hard-wire the plug-in cards together, because the 707's analog backplane automatically carries the signals from one card to another.

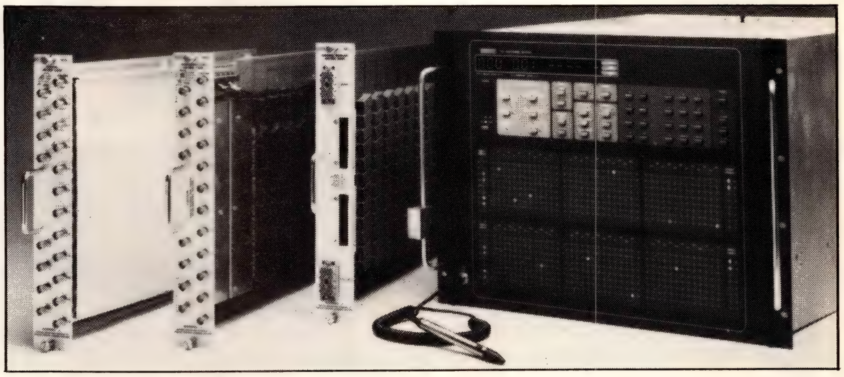
The 707 has a front-panel LED matrix display that represents the cross points on the circuit under test. It also has a continuous switch-status display, so you can determine the status of a relay by glancing at the panel. The light-pen user interface lets you change the state of a relay simply by touching the front panel with the pen. This method reduces both the setup time and the potential for errors.

The Model 707 costs $3500. The light-pen interface sells for $250, and prices for the plug-in cards range from $800 for the universal adapter card to $4900 for the semiconductor matrix card.

—J D Mosley

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400.

Circle No 698



Besides providing a light-pen user interface *that simplifies testing, the Model 707's front-panel LED matrix display lets you note the status of as many as 2880 cross points at a glance.*

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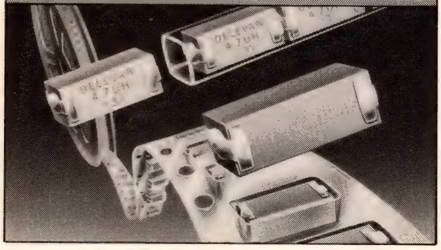

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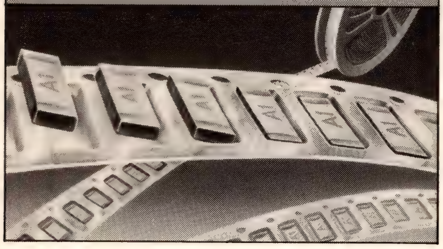

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CIRCLE NO 86

PRODUCT UPDATE

Analog-signal multiplexer plugs into Macintosh II

The Amux-64 card provides analog-signal-multiplexing capability for the vendor's NB-MIO-16 multifunction data-acquisition card for the Apple Macintosh II. The multiplexer card resides in a card cage and connects via a cable to the data-acquisition card, which resides in the Macintosh II.

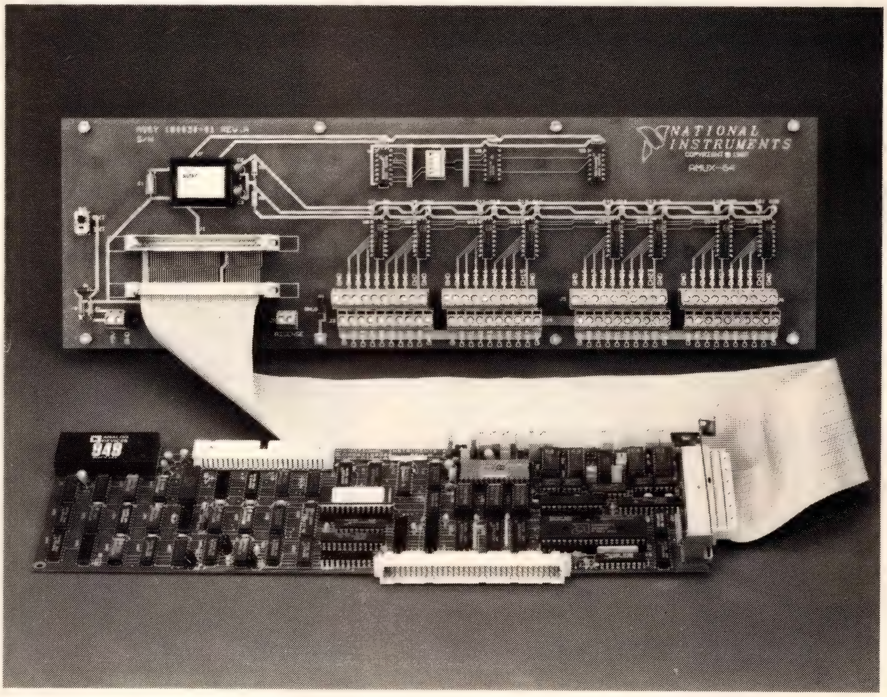
The multiplexer card provides 16 separate 4:1 analog-multiplexer circuits and can multiplex as many as 64 single-ended or 32 differential inputs. The NB-MIO-16 card provides 16 analog-input channels, a 12-bit A/D converter capable of rates as fast as 100k samples/sec, two multiplying 12-bit D/A converters, eight digital I/O lines, and three independent 16-bit counter/timers. You can daisy-chain as many as four Amux-64 cards, thus allowing the NB-MIO-16 to measure as many as 256 single-ended analog inputs simultaneously.

Each Amux-64 card has two 50-pin, male DIN connectors for connecting ribbon cables. One cable connects directly to the I/O connector of the NB-MIO-16 card, which plugs into the chassis of the host computer. You can use the other connector to daisy-chain multiple Amux-64 cards. The Amux-64 sells for $695. Prices for the NB-MIO-16 vary from $1195 to $1495, depending on the A/D-converter speed.

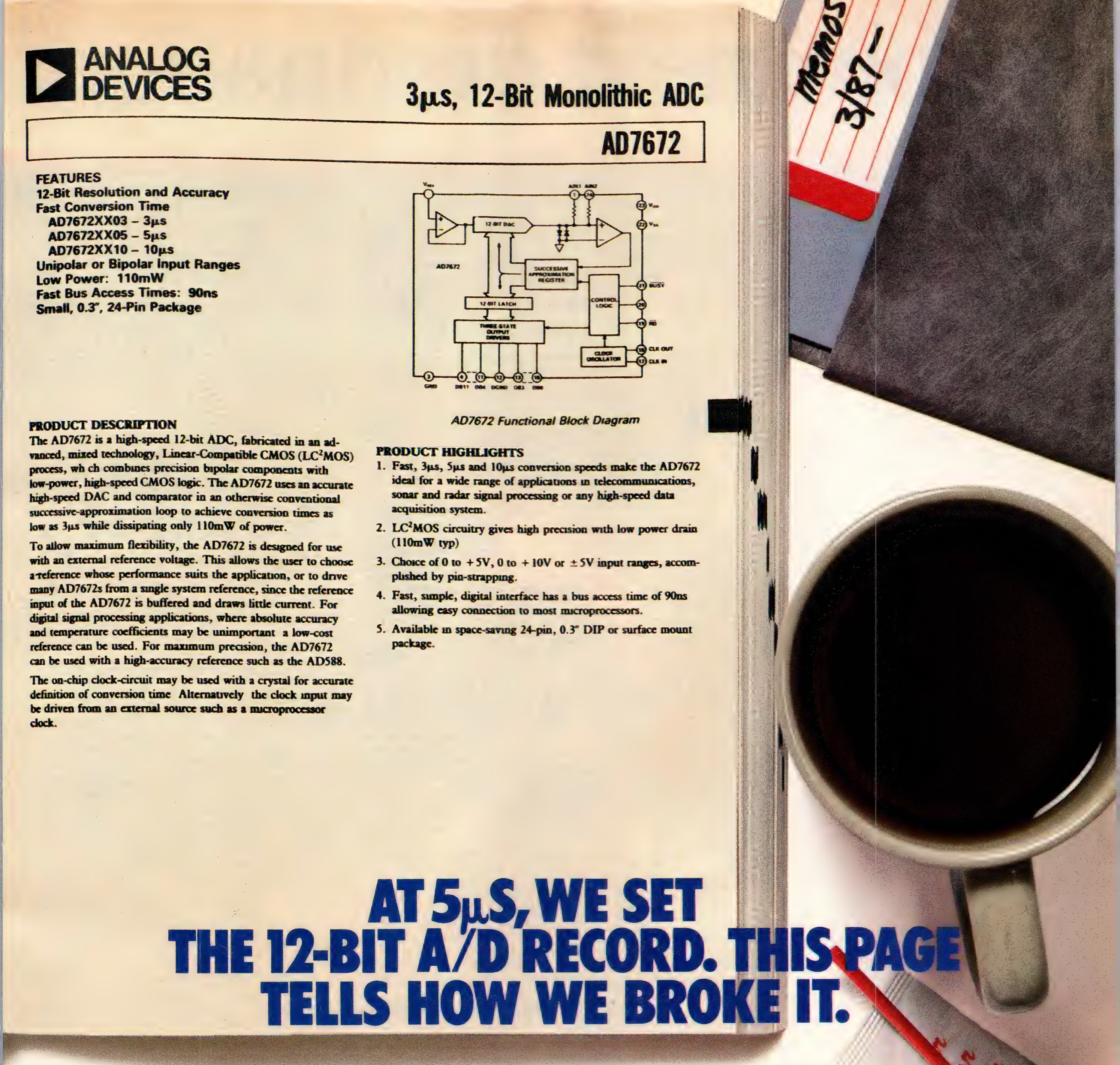
—J D Mosley

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (800) 433-3488. TLX 756737.

Circle No 697



Daisy-chaining as many as four *Amux-64 analog-signal-multiplexer cards to the NB-MIO-16 data-acquisition card lets your Macintosh II measure as many as 256 single-ended analog signals simultaneously.*



ANALOG DEVICES

3μs, 12-Bit Monolithic ADC

AD7672

FEATURES
12-Bit Resolution and Accuracy
Fast Conversion Time
AD7672XX03 – 3μs
AD7672XX05 – 5μs
AD7672XX10 – 10μs
Unipolar or Bipolar Input Ranges
Low Power: 110mW
Fast Bus Access Times: 90ns
Small, 0.3", 24-Pin Package

AD7672 Functional Block Diagram

PRODUCT DESCRIPTION

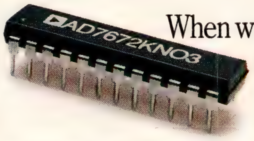
The AD7672 is a high-speed 12-bit ADC, fabricated in an advanced, mixed technology, Linear-Compatible CMOS (LC^{2}MOS) process, which combines precision bipolar components with low-power, high-speed CMOS logic. The AD7672 uses an accurate high-speed DAC and comparator in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3μs while dissipating only 110mW of power.

To allow maximum flexibility, the AD7672 is designed for use with an external reference voltage. This allows the user to choose a reference whose performance suits the application, or to drive many AD7672s from a single system reference, since the reference input of the AD7672 is buffered and draws little current. For digital signal processing applications, where absolute accuracy and temperature coefficients may be unimportant a low-cost reference can be used. For maximum precision, the AD7672 can be used with a high-accuracy reference such as the AD588.

The on-chip clock-circuit may be used with a crystal for accurate definition of conversion time Alternatively the clock input may be driven from an external source such as a microprocessor clock.

PRODUCT HIGHLIGHTS

1. Fast, 3μs, 5μs and 10μs conversion speeds make the AD7672 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any high-speed data acquisition system.
2. LC^{2}MOS circuitry gives high precision with low power drain (110mW typ)
3. Choice of 0 to +5V, 0 to +10V or ±5V input ranges, accomplished by pin-strapping.
4. Fast, simple, digital interface has a bus access time of 90ns allowing easy connection to most microprocessors.
5. Available in space-saving 24-pin, 0.3" DIP or surface mount package.



When we introduced our AD7572, it set the monolithic 12-bit A/D conversion speed record at 5μs. Now, our AD7672 establishes a new record with an even faster conversion time of only 3μs.

The AD7672 reaches this blazing speed with only 110mW of power dissipation because, like the AD7572, it's manufactured on an advanced merged bipolar/CMOS process.

The 90ns bus access time of the AD7672 affords easy interfacing with most microprocessors, while the +5V and –12V nominal power supply voltages allow its use in PC and modem designs. All this is available in a narrow 0.3″ DIP or a surface mount package, so whatever your application, the AD7672 won't take up much space.

The AD7672 also features unipolar or bipolar analog inputs that are selected by pin-strapping. This lets you avoid external circuitry for input range changing.

For more information on how the AD7672 can speed up your designs, contact the Analog Devices office nearest you.

ANALOG DEVICES

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 559-2037; Colorado: (303) 590-9952; Maryland: (301) 992-1994; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; Washington: (206) 251-9550; Austria: (222) 885504; Belgium: (3) 237 1672; Denmark: (2) 845800; France: (1) 4687-34-11; Holland: (1620) 81500; Israel: (052) 28995; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (932) 232222; West Germany: (89) 570050

CIRCLE NO 62

Your next destination:

The ACL Computer Age.

The future belongs to computers and peripherals built with RCA Advanced CMOS Logic (ACL).

The pressure is on to make your systems smaller, faster, cheaper.

Some of your competitors are doing just that by incorporating ACL into their new designs. If you want to stay on the fast track, you can't afford not to consider ACL for your new designs.

The computer of the future.

Imagine a computer with power dissipation so low you could eliminate all cooling systems. Or design a sealed system to prevent dust problems.

And get dramatically improved reliability, thanks to the far lower heat generated. As well as far smaller system size.

You'd also be able to use it in a far wider operating temperature range (-55°C to +125°C). Even in high-noise environments.

FAST* speed, CMOS benefits.

Advanced CMOS Logic gives you high speed (less than 3ns propagation delay with our AC00 NAND gate) and 24 mA output drive current.

But unlike FAST, it gives you a whole new world of design opportunity for computers, peripherals, telecommunications and other speed-intensive applications.

ACL dissipates less than 1/8 Watt while switching, compared to 1/2 Watt for a FAST IC (octal transceiver operating at 5 MHz). And quiescent power savings are even more dramatic: ACL idles at a small fraction of the power of a FAST IC.

In addition, ACL offers balanced propagation delay, superior input characteristics, improved output source current, low ground bounce and a wider operating supply voltage range.

Latch-up and ESD protection, too.

Latch-up concern is virtually eliminated, because ACL uses a thin epitaxial layer which effectively shorts the parasitic PNP transistor responsible for SCR latch-up.

And a dual diode input/output circuit provides ESD protection in excess of 2KV.

A broad and growing product line.

Our line already includes over 100 of the most popular types (SSI, MSI and LSI). More are coming soon. And many are available in High-Rel versions.

All this at FAST prices.

Our ACL line is priced comparably to FAST. So you get better performance at no extra cost. Why wait, when your competition is very likely designing its first generation of ACL products right now?

Get into the passing lane, with RCA ACL from the CMOS leader: GE Solid State. Free test evaluation kits are available for qualified users. Kits must be requested on your company letterhead. Write: GE Solid State, Box 2900, Somerville, NJ 08876.

For more information, call toll-free 800-443-7364, extension 24. Or contact your local GE Solid State sales office or distributor.

*FAST is a trademark of Fairchild Semiconductor Corp.

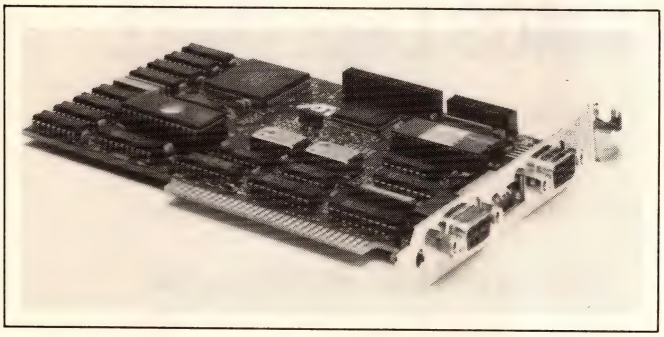
In Europe, call: Brussels, (02) 246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

GE Solid State

GE/RCA/Intersil Semiconductors
Three great brands. One leading-edge company.

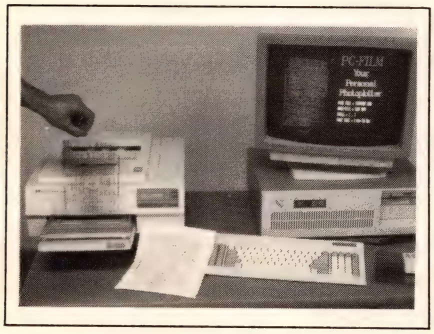
READERS' CHOICE

Of all the new products covered in EDN's **January 7, 1988,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **January 7, 1988,** issue, or use EDN's Express Request service.



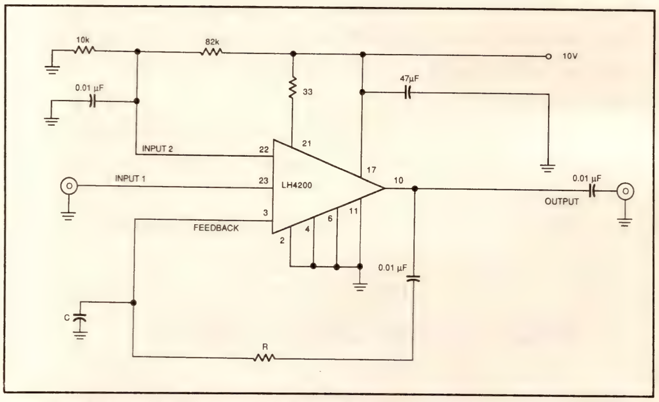
◄ GRAPHICS CARD

The VIP video graphics adapter (VGA) card works with the IBM PC, PC/XT, PC/AT, PS/2 Model 30, Compaq Portable PC, and compatibles. It can display all 17 VGA modes on analog monitors (pg 228).
ATI Technologies Inc.
Circle No 604



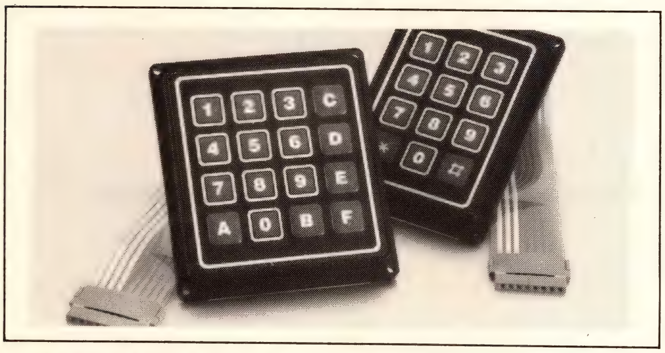
▲ PHOTO-PLOT SYSTEM

The PC-Film photo-plotting package provides a rasterizer card that plugs into your IBM PC or compatible and software that interfaces the system to a 300-dot/in. laser printer (pg 255).
CAD Solutions Inc.
Circle No 605



▲ HYBRID AMPLIFIER

The LH4200 is a general-purpose 500-kHz to 1-GHz amplifier that includes internal decoupling capacitors to simplify its use (pg 103).
National Semiconductor Corp.
Circle No 602



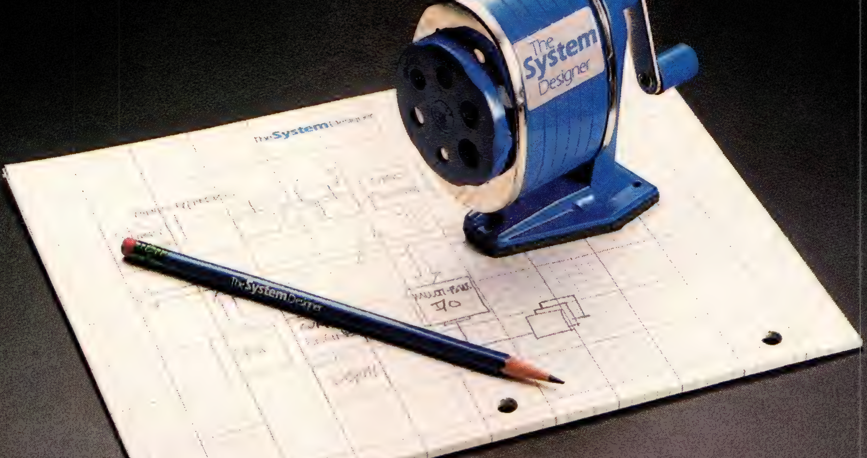
▲ MEMBRANE KEYPADS

The Series 4000 membrane keypads are available in 4×4 and 3×4 arrays with embossed, detented, or flat nontactile keys (pg 215).
C&K Components Inc.
Circle No 603

CALCULATORS

The HP-27S calculator offers both scientific and financial functions to aid the engineering manager who must do engineering design as well as figure out budgets. The HP-28S, an upgrade of the HP-28C, has 32k bytes of user RAM and an augmented user interface (pg 106).
Hewlett-Packard Co.
Circle No 601

This year, you'll hear a lot of claims that "systems" design automation has arrived.



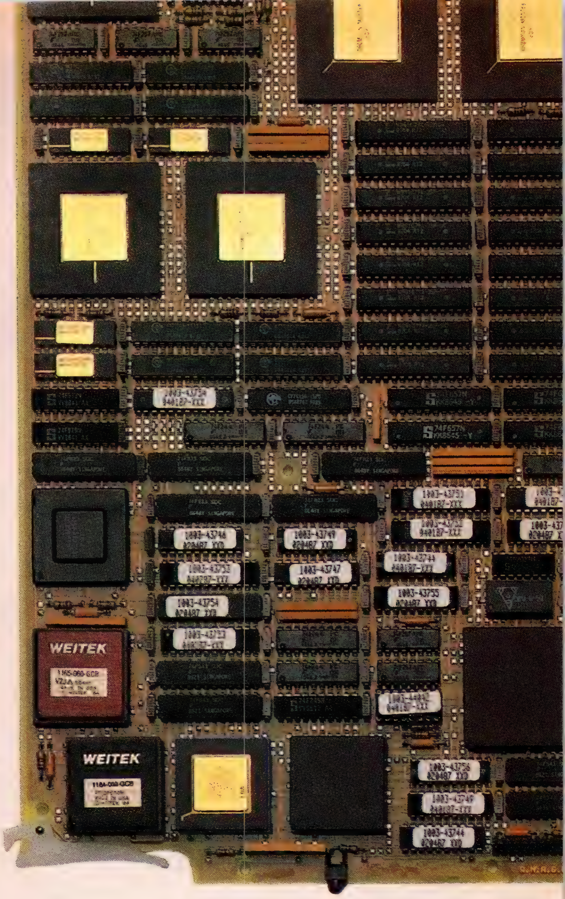
At Mentor Graphics, we
And so do our customers.

Skeptical about "systems" electronic design automation?

You should be. Because in many cases, it's a triumph of form over content. Look behind the facade of so-called "systems" design automation tools, and you'll find little substance, if any.

Buy into this kind of systems design methodology and you're participating in a very costly experiment. With highly uncertain results.

know better.



This 32-bit processor board was designed and simulated on Mentor Graphics workstations by Sequent for its multi-processor Symmetry computer system. It contains over 175 IC components including 80386 processors, a 14,000-gate standard cell and two 10,000-gate arrays. By simulating at the board level, Sequent was able to bypass breadboarding and proceed directly to fabrication prototype.

They preach. We practice.

There's only one practical yardstick for evaluating a systems design solution. And that's how many successful products it has produced.

Apply this measure and the field narrows dramatically. Essentially, down to a single vendor.

Mentor Graphics.

For over five years, our customers have been turning out sophisticated board products with our EDA tool set. Repeatedly. Like Sequent Computer Systems which in 1987 designed and simulated a 32-bit processor board with over 175 chips, including three ASICs, on Mentor Graphics workstations. From design start to diagnostic firmware verification and fabrication prototype in just seven months.

Test their claims.

Many "systems" design automation vendors have a tendency to bypass the obvious and dwell on the esoteric. And for good reason. Most have gaping holes in their product offering. Some interesting (and essential) questions that you should ask vendors:

Does your tool set have a common database and user interface? Does it extend from design definition through to PCB layout and output to manufacturing?

Do you have more ASIC libraries supported on your workstation than any other EDA vendor? Can you include ASICs in board simulations?

Are your tools capable of managing over 1000-page product documentation projects from start to finish?

Have you integrated mechanical packaging and analysis into the electronic design and layout process?

Anything less than a perfect score is a total loss. And a perfect score does not mean just a check in every box. Each item must be backed with the production-proven performance only Mentor Graphics can provide.

Experience makes the difference.

When we speak about systems design automation, we speak from experience. We have the largest customer base in the electronic design automation industry. And with good reason. Some 70% are repeat customers who are gaining genuine value from our products and expanding their competitive advantage.

Our long-term partnership with these customers allows us to continually refine our tools in a very pragmatic and innovative manner. With Mentor Graphics, you get productivity instead of speculation.

To be continued.

So much for the present. We're already developing new systems EDA tools that will extend to every dimension of electronic product development. From high-level systems descriptions to CASE. It's what our customers expect. It's what we'll deliver.

It's all part of a vision unique to Mentor Graphics, the leader in electronic design automation. Let us show you where this vision can take you.

Call us toll-free for an overview brochure and the number of your nearest sales office.

Phone 1-800-547-7390
(in Oregon call 284-7357).

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Mentor Graphics®

Your ideas. Our Experience.

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	7	36	36	21	0	0	7.3	5.7
Pot-Core	0	33	47	20	0	0	7.8	8.2
Laminate (power)	0	40	30	30	0	0	8.3	7.8
CONNECTORS								
Military panel	0	0	63	37	0	0	10.8	12.2
Flat/Cable	10	55	20	15	0	0	5.6	5.3
Multi-pin circular	7	14	43	36	0	0	9.4	8.0
PC (2-piece)	8	23	54	15	0	0	7.4	8.0
RF/Coaxial	17	44	28	11	0	0	5.3	8.1
Socket	17	52	22	9	0	0	4.7	6.0
Terminal blocks	14	50	23	13	0	0	5.4	5.4
Edge card	5	52	33	10	0	0	5.7	6.3
D-Subminiature	9	57	26	8	0	0	5.1	6.6
Rack & panel	7	43	36	14	0	0	6.4	8.6
Power	0	72	14	14	0	0	5.5	11.2
PRINTED CIRCUIT BOARDS								
Single-sided	0	68	21	11	0	0	5.4	4.7
Double-sided	0	56	37	7	0	0	5.8	6.0
Multi-layer	0	29	58	13	0	0	7.5	7.4
Prototype	4	79	8	9	0	0	4.3	3.4
RESISTORS								
Carbon film	26	45	23	6	0	0	4.2	3.0
Carbon composition	35	34	24	7	0	0	4.0	4.3
Metal film	20	45	32	3	0	0	4.4	4.3
Metal oxide	12	59	13	6	0	0	4.6	5.2
Wirewound	4	31	31	34	0	0	8.8	7.2
Potentiometers	7	44	41	4	4	0	6.1	5.2
Networks	10	40	35	15	0	0	6.3	6.6
FUSES	30	40	20	10	0	0	4.4	1.8
SWITCHES								
Pushbutton	17	48	13	22	0	0	5.8	3.9
Rotary	4	50	33	13	0	0	6.1	5.5
Rocker	15	50	20	15	0	0	5.4	5.5
Thumbwheel	6	44	19	31	0	0	7.7	5.7
Snap action	0	56	28	16	0	0	6.5	5.3
Momentary	5	58	16	21	0	0	6.3	5.0
Dual in-line	0	50	36	14	0	0	6.6	7.8
WIRE AND CABLE								
Coaxial	17	63	12	8	0	0	4.2	2.8
Flat ribbon	11	48	30	11	0	0	5.5	3.8
Multiconductor	14	52	29	5	0	0	4.6	3.5
Hookup	43	32	21	4	0	0	3.2	2.9
Wire wrap	38	25	31	6	0	0	4.2	2.2
Power cords	13	54	12	21	0	0	5.9	10.8
POWER SUPPLIES								
Switcher	4	44	26	26	0	0	7.4	7.2
Linear	0	41	35	24	0	0	7.7	6.6
CIRCUIT BREAKERS	6	35	29	30	0	0	8.0	8.3
HEAT SINKS	15	50	23	12	0	0	5.1	4.7
RELAYS								
General purpose	19	43	14	24	0	0	6.1	4.3
PC board	20	30	20	30	0	0	7.2	5.7

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
Dry reed	0	46	15	39	0	0	8.6	7.5
Mercury	0	43	14	43	0	0	9.1	4.4
Solid state	0	36	29	35	0	0	8.9	6.5
DISCRETE SEMICONDUCTORS								
Diode	37	15	27	12	6	3	7.0	3.8
Zener	32	25	18	14	7	4	7.3	4.7
Thyristor	12	29	24	29	6	0	8.8	7.2
Small signal transistor	24	19	33	19	5	0	7.4	4.3
MOSFET	12	29	18	29	6	6	10.2	7.0
Power, bipolar	6	47	13	20	7	7	9.3	6.4
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	10	19	33	33	5	0	9.6	6.8
CMOS	11	36	36	14	3	0	7.1	6.4
TTL	29	17	38	12	4	0	6.5	5.8
LS	24	36	24	12	4	0	5.9	5.2
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	15	23	31	23	8	0	8.7	6.7
OP amplifier	25	33	21	17	4	0	6.3	7.1
Voltage regulator	15	40	20	20	5	0	7.2	6.6
MEMORY CIRCUITS								
RAM 16k	15	25	25	20	15	0	9.7	7.8
RAM 64k	13	35	22	17	13	0	8.8	7.7
RAM 256k	12	18	35	23	12	0	10.0	9.5
RAM 1M-bit	8	17	17	42	16	0	12.5	11.8
ROM/PROM	7	27	20	33	13	0	11.0	8.2
EPROM 64k	5	38	19	29	9	0	9.5	7.8
EPROM 256k	9	30	26	26	9	0	9.3	8.4
EPROM 1M-bit	7	13	33	34	13	0	11.6	9.4
EEPROM 16k	6	24	29	29	12	0	10.6	8.3
EEPROM 64k	11	17	33	22	17	0	10.9	8.3
DISPLAYS								
Panel meters	8	50	17	25	0	0	6.7	6.0
Fluorescent	11	45	11	22	11	0	8.5	11.1
Incandescent	22	45	0	33	0	0	6.5	8.8
LED	15	30	25	25	5	0	8.1	5.6
Liquid crystal	0	29	29	35	7	0	10.5	11.3
MICROPROCESSOR ICs								
8-bit	22	17	39	17	5	0	7.6	6.5
16-bit	11	17	39	28	5	0	9.3	6.7
32-bit	7	26	47	20	0	0	7.6	7.1
FUNCTION PACKAGES								
Amplifier	20	30	30	20	0	0	6.4	6.4
Converter, analog to digital	13	20	40	20	7	0	8.6	8.2
Converter, digital to analog	17	17	33	25	8	0	9.2	8.0
LINE FILTERS	0	45	22	22	11	0	9.4	6.8
CAPACITORS								
Ceramic monolithic	22	37	22	19	0	0	5.8	5.5
Ceramic disc	22	44	19	15	0	0	5.1	5.6
Film	32	41	9	18	0	0	4.8	6.0
Aluminum electrolytic	30	41	18	7	4	0	4.8	6.4
Tantalum	28	31	21	17	3	0	6.2	5.9
INDUCTORS	0	40	30	20	10	0	9.3	7.7

Source: *Electronics Purchasing* magazine's survey of buyers

Get it out of your system.

Mentor Graphics presents a one-day technical seminar on applying electronic design automation to board and systems development.

With the advent of 32-bit processors, ASICs with VLSI densities, and surface mount PCB technology, board design is reaching an unprecedented level of complexity. This one-day seminar will show you how Electronic Design Automation (EDA) can help you handle this mounting complexity – without disrupting your current methodologies.

Who should attend.

Engineering managers, design engineers, project leaders, and any other technical professionals who are concerned with developing engineering strategies for board design and layout.

What you'll learn.

You'll learn how EDA can help you produce better designs and substantially accelerate board design and analysis through advanced design definition and simulation tools. And how other engineering departments have already tackled complex designs while also cutting months off their design cycles with EDA.

The seminar will cover a wide range of topics and include the actual experiences of board and systems designers who have successfully adopted EDA to a broad array of projects. Among other issues, it will examine:

- New approaches to absorbing the steady increase in design complexity.
- Logic verification of board designs with ASICs and PLDs.
- Techniques for addressing timing problems.
- Handling SMT packaging problems efficiently.
- Firmware debugging with software-based breadboards.
- Controlling placement and routing early in the design process.
- Handing off a more testable product to test engineering.
- Comparisons of traditional prototype tools with electronic design automation tools.

You'll also hear a variety of leading systems designers discuss real-world design techniques that maximize the value of EDA tools. Extensive audio/visual aids will be employed and you'll also be provided with a designer's casebook to capture many of the examples provided throughout the day.

How to register.

Call the seminar coordinator at the phone numbers in the cities listed below. But hurry, because space is limited. There is a $65 charge, which includes all materials and lunch. PLEASE NOTE: Checks or money orders postmarked after April 8 will be returned.

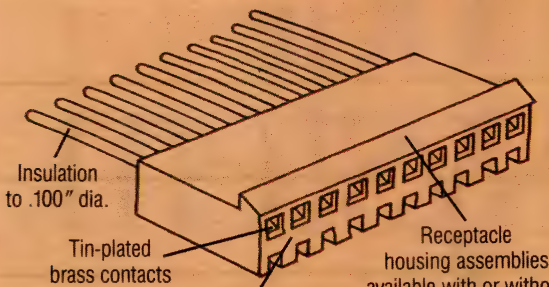
Where and When.

April 19:	Chicago	Call 312-490-0230
	San Jose	Call 408-436-5494
April 22:	Minneapolis	Call 612-541-0776
	Los Angeles	Call 213-640-9525
April 26:	Paramus NJ	Call 201-845-0550
	Orange County	Call 714-770-1573
April 28:	Boston	Call 617-891-3341
April 29:	Dallas	Call 214-233-9897

Mentor Graphics®

Your ideas. Our Experience.

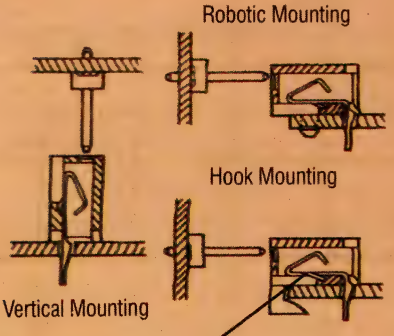
SINGLE LEAF .156 CONNECTORS


Insulation to .100″ dia.
Tin-plated brass contacts
1 to 24 positions. Wire sizes 24 to 18 AWG.
Receptacle housing assemblies available with or without locking ramp.

Crimp-termination, wire-to-board and board-to-board connectors mate with pin half or MTA-156 Series post headers. Housings molded from flame-retardant material to meet UL 1410 Standard for Television and Video Products. Contacts rated 6.5 amps, 250 VAC.

BOARD TO BOARD RECEPTACLES

Right angle or vertical receptacle housing assemblies. Hook or robotic mounting styles. 3 to 15 positions.


Robotic Mounting
Hook Mounting
Vertical Mounting
Phosphor bronze contacts plated tin or selective gold over nickel

MTA-100 MASS TERMINATION ASSEMBLIES

Closed end or feed-thru housings
Contact accepts solid, stranded, or fused stranded wires

Meet our

They've gone everywhere. And gotten into everything.

And proven themselves in literally millions of applications.

Our MTA assemblies have been problem solvers since we introduced them. They reflect a business attitude we have—that the best way to win a customer is to help. With big concerns like availability. Or simple concerns like having a question, and wanting an answer.

Test our reflexes.

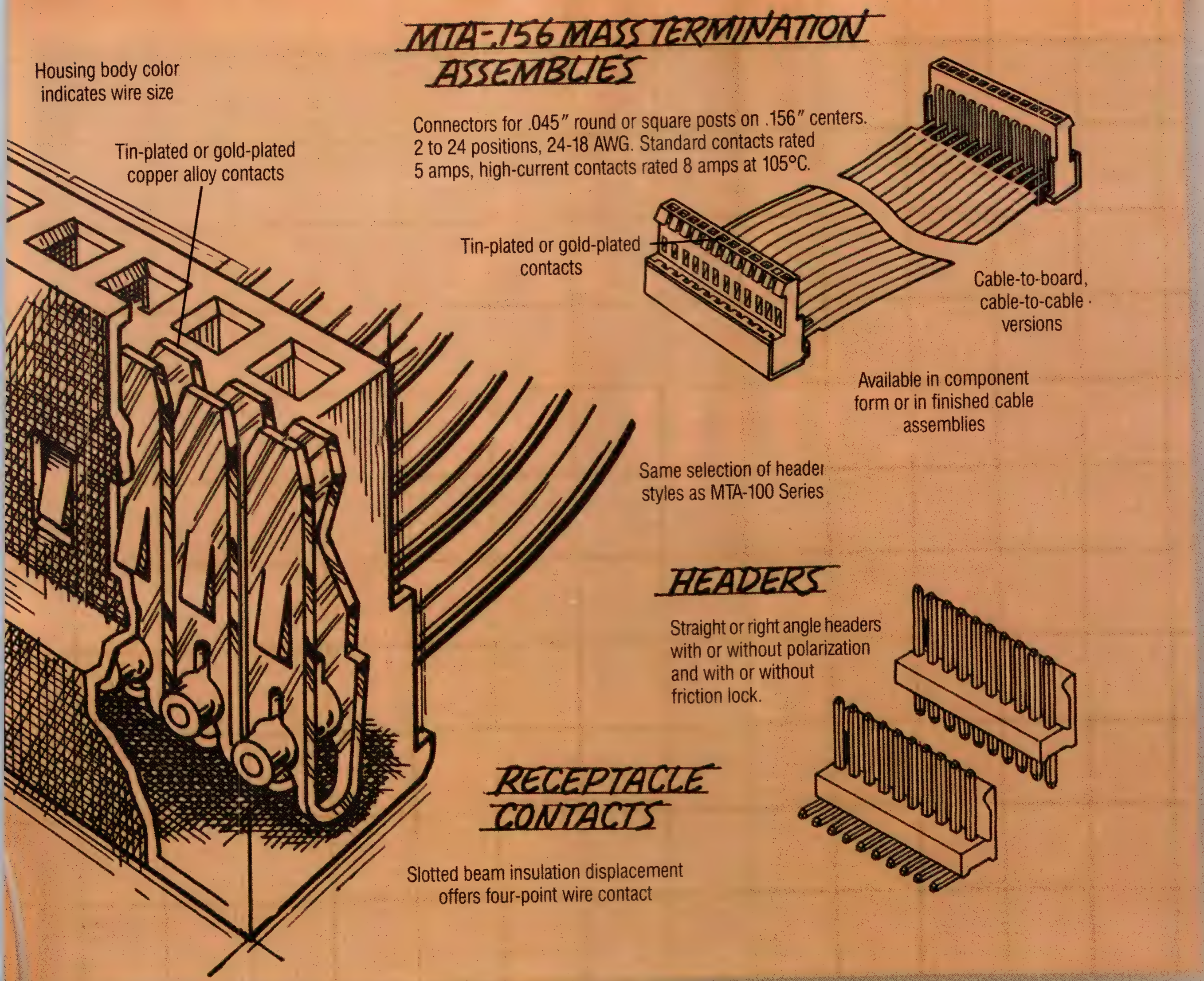
Our real job is to be the kind of company you want to do business with.

So we take availability seriously, and make AMP products available the way *you* need them. From worldwide manufacturing and stocking to our nationwide network of AMP Authorized Distributors, we offer the source that suits you.

You sometimes need parts in a rush. We've done something about that, too. We've taken our popular industry standard products—including MTA connectors—and stocked up, nationwide.

Your Immediate Shipment Catalog is ready.

For thousands of products from switches to sockets, terminals to coax, and more, our Industry Standard Products Catalog is almost as good


MTA-.156 MASS TERMINATION ASSEMBLIES
Housing body color indicates wire size
Connectors for .045″ round or square posts on .156″ centers. 2 to 24 positions, 24-18 AWG. Standard contacts rated 5 amps, high-current contacts rated 8 amps at 105°C.
Tin-plated or gold-plated copper alloy contacts
Tin-plated or gold-plated contacts
Cable-to-board, cable-to-cable versions
Available in component form or in finished cable assemblies
Same selection of header styles as MTA-100 Series
HEADERS
Straight or right angle headers with or without polarization and with or without friction lock.
RECEPTACLE CONTACTS
Slotted beam insulation displacement offers four-point wire contact

multi-millionaires.

as a warehouse around the corner.

And you can get your copy just by calling our Information Center and asking for it.

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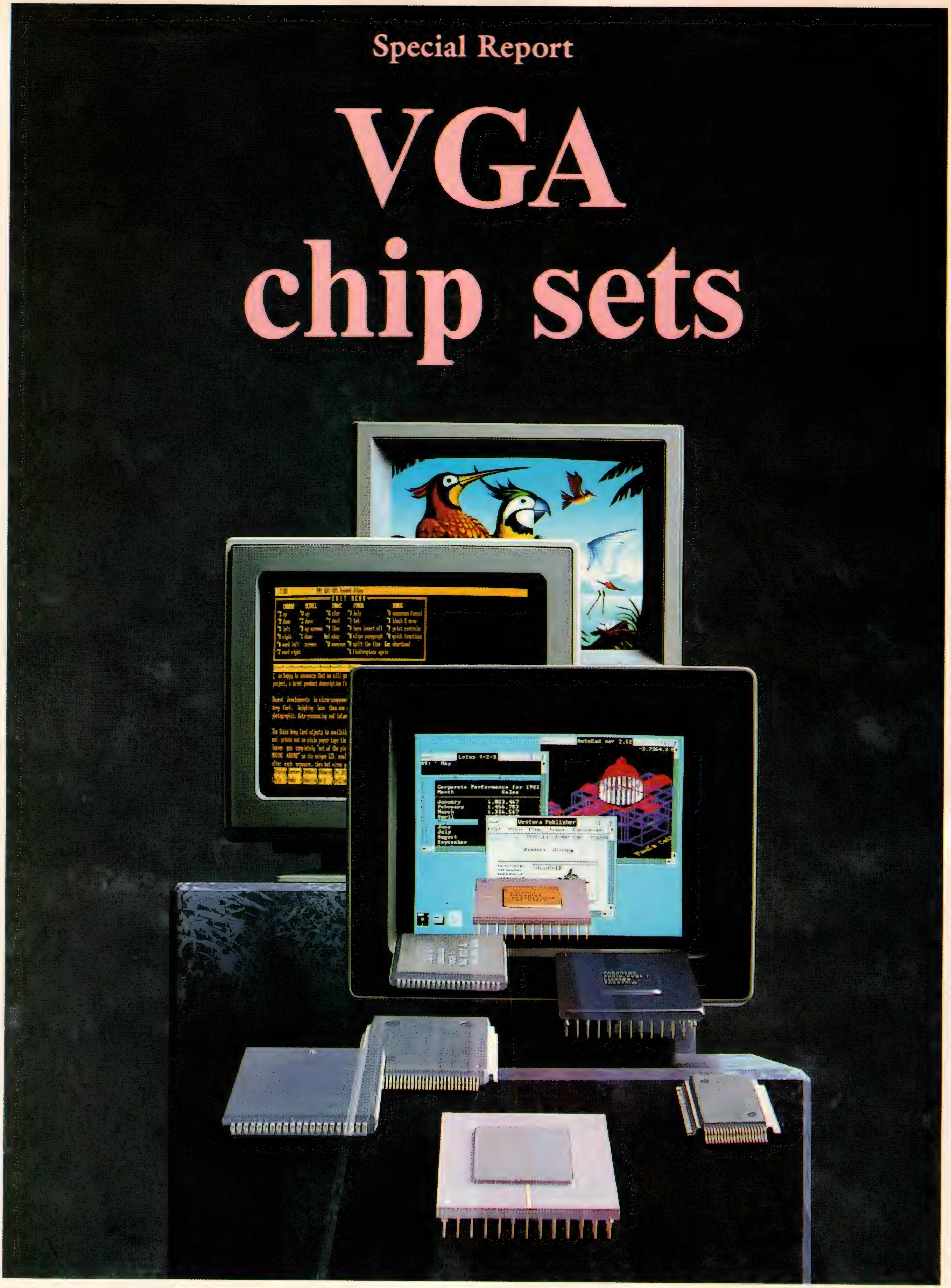
CIRCLE NO 63

Special Report

VGA chip sets



Vendors of graphics chips *are helping you achieve the impressive color-graphics capabilities of IBM's VGA without sacrificing compatibility with existing software. (Photo courtesy Paradise Systems Inc)*

While debating degrees of compatibility with IBM's Video Graphics Array standard, manufacturers of VGA-like chips are attempting to woo designers by offering exotic features and backward compatibility with other IBM display products. Fortunately, the shipping delays and vaporware that had plagued this market have abated.

J D Mosley, *Regional Editor*

IBM's PS/2 Series computers and their Video Graphics Array (VGA) graphics controllers are less than one year old, and already the market is thick with competing versions of the controller that IBM tried to make unclonable. Therefore, designers and programmers who have finally begun to make full use of the colors and resolution provided by IBM's earlier Enhanced Graphics Adapter (EGA) standard must now deal with the VGA. However, debate rages over the pace of the evolution from EGA to VGA.

Although most of IBM's PS/2 computers come with VGA hardware, conversion of IBM PCs and compatible computers to the VGA standard requires users to purchase both a VGA board and an analog monitor, because VGA won't work with the ubiquitous digital monitors that dominate the current PC market. Further, IC manufacturers disagree about the level of VGA compatibility that will be necessary to let an expansion board run VGA software that doesn't yet exist. And some industry observers doubt that the VGA standard offers enough of a performance improvement over EGA to justify the expense of conversion.

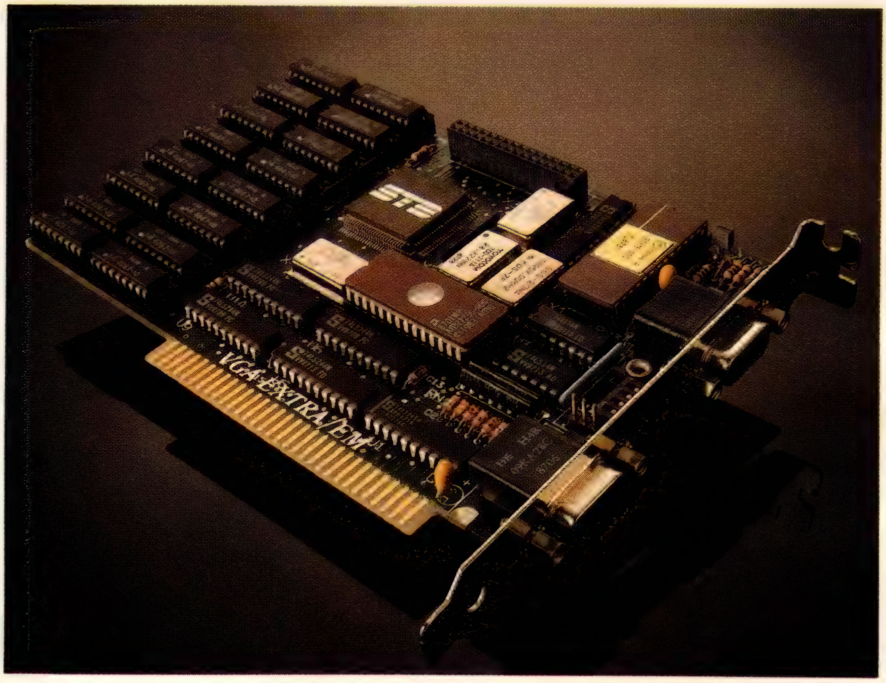
Yet another new standard

When IBM introduced the PS/2 line, the company forced yet another new video standard into the PC market. The mother boards of the PS/2 Series Models 50, 60, and 80 come equipped with a VGA circuit that surpasses the performance of IBM's EGA. Conversely, users of PC-compatible computers must select and purchase graphics boards for their machines and then plug them into expansion slots in the computers' chassis. Besides EGA, PC users can choose from a number of graphics standards, including the Hercules (Berkeley, CA) monochrome graphics controller and IBM's Monochrome Display Adapter (MDA), Color Graphics Adapter (CGA), Professional Graphics Adapter (PGA), and Multicolor Graphics Array (MCGA).

EGA boards provide a selection of 16 simultaneous colors from a palette of 64, with a resolution of 640×350 pixels, on a digital monitor. VGA requires an analog monitor and lets you select 16 colors from a palette of 256, with 640×480-pixel resolution. At a lower resolution of 320×200 pixels, VGA can simultaneously display 256 colors from a palette of 262,144. The analog monitor permits infinitesimal shading gradations, thereby providing spectral variations that digital monitors can't achieve. However, the EGA standard is now more than two years old, and an EGA board's price is about half that of a VGA board's. Moreover, an analog monitor, such as the NEC (Mountain View, CA) Multisync, could add more than $700 to the cost of VGA conversion.

Because companies that purchase the PS/2 line of computers automatically get VGA, they probably will eventually want to standardize their PCs on the VGA specification to prevent software incompatibility problems from surfacing. And the chip manufacturers that have entered the VGA market contend that such com-

Because IBM built its VGA controller into the PS/2 mother board, VGA BIOS is part of the system BIOS—not a separate, easily deciphered entity.



Electing not to get into the chip business, *STB Systems is one graphics-board manufacturer that preferred to use a commercial VGA controller instead of trying to design and debug a semicustom VGA IC.*

panies will create a viable market for plug-in VGA boards.

Availability is a problem

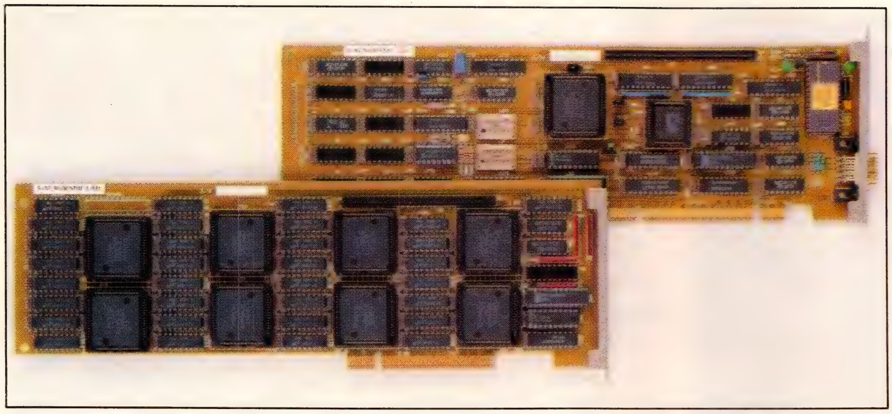
Video Seven, one of the first chip manufacturers to ship ICs that attempt to emulate the VGA, uses two 84-pin packages to house its rendition of IBM's controller. The chip set provides hardware- and software-compatible emulation and has all the control and data registers defined for the VGA, EGA, CGA, MDA, and Hercules graphics controllers. The chip set automatically switches among these graphics standards when it detects software conditions that are unique to each. You can also lock the hardware into a single standard or program the chips to generate a nonmaskable interrupt if a program tries to access hardware features that are unavailable in a particular mode. A new video-RAM version of the chip set costs $50 (10,000).

Because the VGA is a graphics controller and not a processor, display processing occurs in the host computer's CPU. To minimize the wait-state-induced delays that can arise as the CPU's workload increases when accessing video memory, the Video Seven chip set lets you allocate all memory cycles that aren't being used to refresh the display or video memory to process CPU memory requests. And to reduce the software overhead created by mouse-oriented programs such as Microsoft's (Remond, WA) Windows, the chip set includes a hardware-controlled 32×32-pixel graphics cursor.

The chip set's 33-MHz max dot-clock rate provides display resolution as great as 800×600 pixels. A fast dot-clock spec translates into greater display resolution, because the faster the chip can shift pixel data out of the frame buffer, the more time the CPU has for writing graphics data to the frame buffer. The chip set also includes a scratchpad RAM, a BIOS ROM-disable function, a restorable-state function, flicker-free CGA text scrolling, and eight text fonts.

Video Seven also sells its $499 Vega VGA expansion card, which uses the company's chip set to provide VGA compatibility for your PC or compatible computer. The board comes with high-resolution 800×600-pixel drivers for Microsoft's Windows, Autodesk's (Sausalito, CA) AutoCAD, and Lotus's (Cambridge, MA) 1-2-3 graphics. However, you can only display at this resolution if you have a variable-frequency monitor. IBM-compatible analog monitors limit you to a maximum resolution of 640×480. However, the Vega VGA has both analog- and digital-monitor connectors, so you can postpone the decision to upgrade your monitor. The board interfaces with its VGA chip set and the system bus via video RAM instead of dynamic RAM, thereby producing zero-wait-state operation at speeds four times faster than IBM's EGA.

Video Seven's chip set isn't 100% hardware-compati-



If you want to boost the display specs of a PS/2 computer, *you can plug in Gala-Graph's Galaxy Mercury/2 board set to gain zoom windows and resolution as great as 1024×768 for your CAD applications.*

ble with IBM's VGA because of register conflicts between the EGA and VGA standards. To have both on the same chip set, Video Seven elected to provide complete EGA register compatibility and VGA compatibility at the software level. The engineers at Video Seven determined that 100% EGA compatibility would be a major factor influencing VGA-chip consumers until a broad range of software written to the VGA standard appears on the market. In addition, some of IBM's VGA registers remain undocumented, presenting a degree of uncertainty when attempting hardware compatibility with IBM's VGA chip.

In contrast, Paradise Systems chose to design its PVGA1 chip with full VGA hardware compatibility and EGA BIOS-level software compatibility. Citing the danger of system crashes as the primary concern, company officials note that register-dependent programs written to the VGA standard are already commercially available. Furthermore, it isn't unusual for software developers to write programs that bypass the host's software-interface BIOS and directly access the graphics hardware to accelerate program execution.

The PVGA1, which is 81% smaller than IBM's VGA video controller, provides 17 graphics modes and eight alphanumeric modes with resolutions ranging from 320×200 to 1024×768 pixels. This 1.5-μm, 12,000-gate CMOS LSI device comes in either a 100-pin plastic pin-grid array (PGA) or a plastic flat package. Five proprietary graphics modes that Paradise defined for this chip provide resolution greater than the IBM VGA controller allows. Because of the PVGA1's 40-MHz max video clock rate, one mode lets you select from 256 simultaneous colors in a palette of 262,144 colors at a resolution of 640×480 pixels. A monochrome graphics mode permits you to boost resolution to 1024×768 pixels. The chip provides flicker-free operation in all video modes.

The PVGA1's bus interface functions with either an 8- or 16-bit-wide data bus, which makes the chip as much as three times faster than IBM's VGA chip with its 8-bit data bus. The chip also contains six lock-protected I/O registers that you can use to enhance certain video, memory, and address functions contained in IBM's VGA standard. Further, the company claims that a VGA expansion board for a PC or compatible computer would require only 21 components for designers using the PVGA1, instead of 32 components if the IBM VGA were used. A PS/2 mother board based on the Paradise chip would require only 16 components. The $60 (100) PVGA1 comes with a proprietary BIOS.

Paradise has designed two boards based on the PVGA1: The VGA Professional Card and the VGA Plus Card. When compared to the $595 IBM PS/2 Display Adapter, Paradise's $399 VGA Plus Card adds Hercules monochrome compatibility and 132-column support to the IBM card's standard features. The $599 VGA Professional Card includes a 16-bit bus, monochrome graphics resolution reaching 1024×768 pixels, and color graphics featuring 800×600-pixel resolution. The company expects to provide high-resolution drivers for a number of software packages, including Microsoft Windows, Digital Research (Monterey, CA) GEM, and Ashton-Tate (Torrance, CA) Framework, Lotus 1-2-3 and Symphony, AutoCAD, and Xerox (Rochester, NY) Ventura Publisher.

The VGA Professional Card should be available in May; the VGA Plus card should be available now, although driver design delays have postponed quantity shipments of the boards. Customers such as Compaq Computer Corp, however, have acknowledged receipt of volume shipments of the Paradise PVGA1 video controller. In fact, Compaq is now shipping its own $599 VGA controller board for use in its Deskpro and Portable 386 and 286 computers.

It isn't unusual for software developers to write programs that bypass the host's software-interface BIOS and directly access the graphics hardware.

The VGA standard supports analog monitors; *the VGA-compatible chip set from Cirrus Logic lets you display as many as 256 colors with more subtle shading than is possible using the EGA graphics standard and a digital monitor.*

In a maneuver to boost specs for NSI Logic's Enhanced Video Controller (EVC) 415 chip, the company offers three enhancement ICs, one of which is dubbed a "resolution multiplier," which allegedly can double display resolution—that is, the 640×480 mode would appear as 1280×960 pixels. A color-expander chip provides 256 simultaneous colors at resolutions of 640×480 or 800×600 pixels, and a bus-enhancer chip lets 32-bit host computers directly access the EVC 415's 32-bit video bus. Without the bus enhancer, your system interfaces with the EVC 415 via a 16-bit-wide data path.

NSI Logic has graced the chip with such techniques as packed pixel mapping in the video memory array to accelerate screen drawing. Another such technique is the board's 1:1 interleave scheme, called Proprietary Virtual Access Arbitration, which lets the CPU access the chip's video memory on demand. Company officials expect to begin shipping these ICs in volume this month. Pricing begins at less than $20 (OEM).

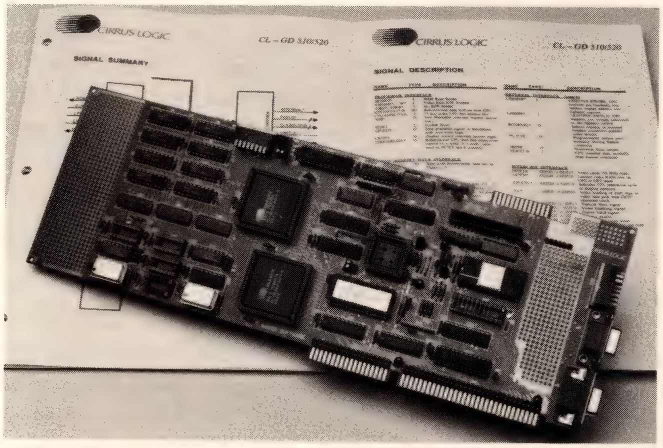
Volume shipments begin

Chips and Technologies is now accepting orders for volume shipments of the company's 2-chip set, which includes the $30.50 (1000) 82C441 VGA chip and the $10 (1000) 82A442 bus-interface chip. They provide a maximum dot-clock rate of 38 MHz for 800×600-pixel resolution in 16 colors. Tseng International Laboratories is also taking orders for volume shipments of a VGA implementation—its ET3000 chip. You can clock this chip to 65 MHz for a display of 1024×768 pixels in 16 colors out of a palette of 256. VGA compatible down to the register level, this IC sells for $45 (OEM).

Package eases design effort

Cirrus Logic, another VGA chip manufacturer, offers a dual-chip set that includes glue logic to simplify board-level design and a sequencer that allows the host CPU more frequent access to the video memory than a single-chip implementation would. This design lets the CL-GD510/CL-GD520 chip set use dynamic RAMs rather than expensive video RAMs to drive high-resolution displays. In addition, the chips include a hardware reconfiguration capability that provides register-level compatibility with both the EGA and VGA standards. When the software indicates EGA or VGA mode, the chips actually enable and disable reserved registers to provide full compatibility.

The hardware provides both a graphics and a text cursor to reduce software overhead and speed application processing by the host. You also get a hardware-driven split screen that provides simultaneous and independent scrolling of two separate text screens. The set also includes an on-chip scratchpad RAM for storage of BIOS and driver software. Backwards compatible with earlier PC-based graphics standards, and supporting both digital and analog monitors, the CL-GD510/CL-GD520 set also includes a host register read-back capability that eliminates any need for shadow registers and permits graphics-controller state saving for



To cut your development time, *you can start your prototype design with this VGA board from Cirrus Logic. It provides room for additional circuitry and gives you access to extra switches, jumpers, and crystal options.*

multitasking applications.

By using two chips instead of one, Cirrus Logic eliminated complex I/O multiplexing to simplify your board design effort. The company also sells a $450 fully functional VGA graphics development board that has extra switches, jumpers, and crystal options as well as space for additional prototyping to help you develop your own custom VGA board. The CL-GD510/CL-GD520 chip set comes in an 84-pin PLCC package and costs $45 (1000).

Boards sport proprietary ICs

Many graphics-board manufacturers have developed their own ASICs instead of relying on the IC houses for commercial chip sets. ATI Technologies, for example, features a proprietary graphics array chip on its VGA Improved Performance (VIP) board. The VIP plugs into IBM PC, PC/XT, and PC/AT or compatible, computers, including portable models and the IBM PS/2 Series Model 30. ATI used CMOS VLSI SMDs to reduce the VIP's chip count and power consumption. The board's 256k bytes of video RAM eliminate any need for supplemental memory modules. The VIP is compatible with both digital and analog monitors, and if you use an analog display with this board, you can display 16 colors at a resolution of 640×480 pixels. This $449 board comes with a 2-year warranty, including parts and labor. The board features software drivers for AutoCAD, GEM, Lotus 1-2-3, Aldus Corp's (Seattle, WA) Pagemaker, Ventura Publisher, and Microsoft Windows.

Another board-level offering is Sigma Designs' $579

COMPARATIVE FEATURES OF REPRESENTATIVE VGA CHIP SETS

MANUFACTURER	PART	DOWNWARD COMPATIBILITY	VGA REGISTER-LEVEL COMPATIBILITY	MAXIMUM DOT-CLOCK RATE (MHz)	ADDITIONAL MODES	AVAILABILITY	PRICE
ATI TECHNOLOGIES	PROPRIETARY	EGA, CGA, MDA, HGC	NO	32	800×560, 132 COLUMNS	NOW (ON $449 VIP BOARD)	N/A (PROPRIETARY)
CHIPS & TECHNOLOGIES	82C441/82A442	EGA, CGA MDA, HGC	YES	38	800×600	NOW	$30.50 & $10 (1000)
CIRRUS LOGIC	CL-GD510/ CL-GD520	EGA, CGA, MDA, HGC	YES	32.5	1056×200, 1056×350, 960×350, 880×480, 800×500, 800×600	NOW	$45 (1000)
GALAGRAPH LTD	PROPRIETARY	MDA, MCGA, HGC	NO	N/A	800×600, 1280×960	NOW (ON $2495 GALAXY MERCURY/2 BOARD)	N/A (PROPRIETARY)
IBM	VGA CONTROLLER	EGA, CGA, MDA, MGCA, HGC	YES	28.5	N/A	NOW (ON $595 PS/2 DISPLAY ADAPTER)	N/A (PROPRIETARY)
NSI LOGIC	EVC 415	EGA, HGC	YES	40	752×410, 800×600, 960×720, 1280×960	NOW	<$20 (OEM)
PARADISE SYSTEMS	PVGA1	EGA, CGA, MDA, MCGA, HGC	YES	40	800×600, 960×780, 1024×768, 1056×344, 1056×770, 1188×350	NOW	$60 (100)
SIGMA DESIGNS	PROPRIETARY	EGA, CGA, MDA, MCGA, HGC	YES	65	800×600, (1024×768 & 8514/A OPTIONAL)	NOW (ON $579 VGA/X BOARD)	N/A (PROPRIETARY)
TSENG LABORATORIES	ET3000	EGA, CGA, MDA, HGC	YES	65	1024×768, 960×720, 800×600, 160 COLUMNS	NOW	$45 (OEM)
VIDEO SEVEN	VGA CHIP SET	EGA, CGA, MDA, HGC	NO	33	800×600	NOW	$50 (OEM)

LEGEND: HGC=HERCULES MONOCHROME GRAPHICS CONTROLLER
MDA=IBM MONOCHROME DISPLAY ADAPTER
CGA=IBM COLOR GRAPHICS ADAPTER
MCGA=IBM MULTICOLOR GRAPHICS ARRAY

Many graphics-board manufacturers have developed their own ASICs instead of relying on the IC houses for commercial chip sets.

VGA/X board. Teamed with an X-Plus upgrade option that lets you display 16 colors at a resolution of 1024×768 pixels, the enhanced board with its proprietary VGA chip will also provide software compatibility with IBM's 8514/A display adapter, which boasts 256-simultaneous-color display at a resolution of 1024×768 pixels. IBM's 8514/A board sells for $1290, and its 16-in., interlaced, analog monitor costs an additional $1550. The X-Plus upgrade will cost less than $200; OEM quantities should be available by the end of this month. The VGA/X board and a $399 version, called the VGA/H, provide register-level compatibility with IBM's VGA, as well as downward compatibility with the older PC-graphics standards. The VGA/X features software drivers for AutoCAD, GEM, Lotus 1-2-3, Ventura Publisher, and Microsoft Windows.

Leave Si to the chip designers

STB Systems sells a board, called the VGA Extra/EM, that sports a Tseng Laboratories chip that emulates VGA at the register level. VGA enhancements found on this board—which the manufacturer is currently shipping in volume—include a 1024×768-pixel mode with 16 simultaneous colors; 256 simultaneous colors in resolutions of either 960×720, 800×600, or 640×480 pixels; and a 160-column×55-line text mode that is particularly useful for spreadsheet production and terminal emulation. You can order this board with 256k bytes of video RAM for $495 or with 512k bytes for $595. The VGA Extra/EM also has an interlaced video mode for use with IBM's 8514/A display monitor.

Similar specs are offered by Genoa Systems for its SuperVGA HiRes board—another board that uses the Tseng Laboratories controller chip. The SuperVGA lets you display 256 colors at 800×600-pixel resolution. An optional 1024×768-pixel mode offers 16 simultaneous colors. The $695 board provides 512k bytes of video RAM. A $495 version, called the SuperVGA, presents 16-color, 800×600- and 640×480-pixel modes; a 256-color, 320×200-pixel mode; and compatibility with the

Manufacturers of VGA ICs and boards

For more information on VGA ICs and boards such as those described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

ATI Technologies Inc
3761 Victoria Park Ave
Scarborough, Ontario
Canada, M1W 3S2
(416) 756-0711
TLX 069666
Circle No 650

Chips and Technologies Inc
3050 Zanker Rd
San Jose, CA 95134
(408) 434-0600
Circle No 651

Cirrus Logic Inc
1463 Centre Pointe Dr
Milpitas, CA 95035
(408) 945-8300
Circle No 652

Compaq Computer Corp
20555 FM 149
Box 692000
Houston, TX 77269
(713) 370-0670
Circle No 653

GalaGraph Ltd
Box 32127
Tel Aviv 61321 Israel
(972-3) 751-4425
TLX 361539
Circle No 654

GalaGraph Ltd
c/o Electrograph Sales Inc
1568 Ocean Ave
Bohemia, NY 11716
(516) 563-1320
Circle No 655

Genoa Systems Corp
73 E Trimble Rd
San Jose, CA 95131
(408) 432-9090
Circle No 656

IBM
Old Orchard Rd
Armonk, NY 10504
Phone local office
Circle No 657

NSI Logic Inc
257-B Cedar Hill Rd
Marlboro, MA 01752
(617) 460-0717
Circle No 658

Paradise Systems Inc
99 S Hill Dr
Brisbane, CA 94005
(415) 468-7300
Circle No 659

Quadram
1 Quad Way
Norcross, GA 30093
(404) 923-6666
TWX 810-766-4915
Circle No 660

Sigma Designs Inc
46501 Landing Parkway
Fremont, CA 94538
(415) 770-0100
FAX 415-770-0110
Circle No 661

STB Systems Inc
1651 N Glenville
Suite 210
Richardson, TX 75081
(214) 234-8750
Circle No 662

Tseng International Laboratories
10 Pheasant Run
Newtown, PA 18940
(215) 968-0502
Circle No 663

Video Seven Inc
46335 Landing Parkway
Fremont, CA 94538
(415) 656-7800
Circle No 664

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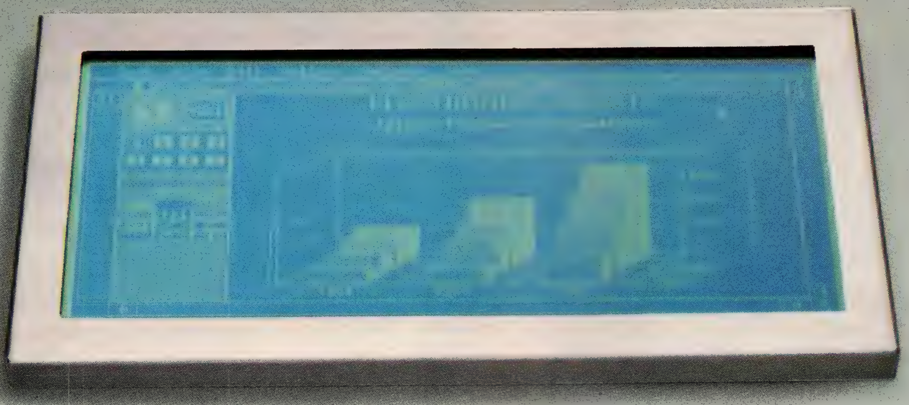

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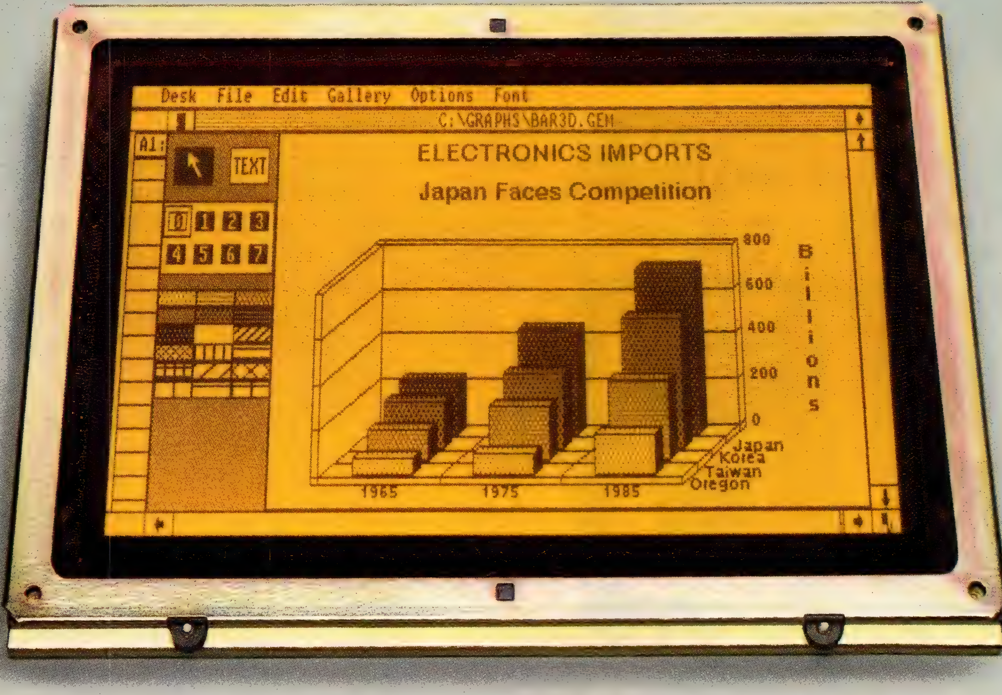

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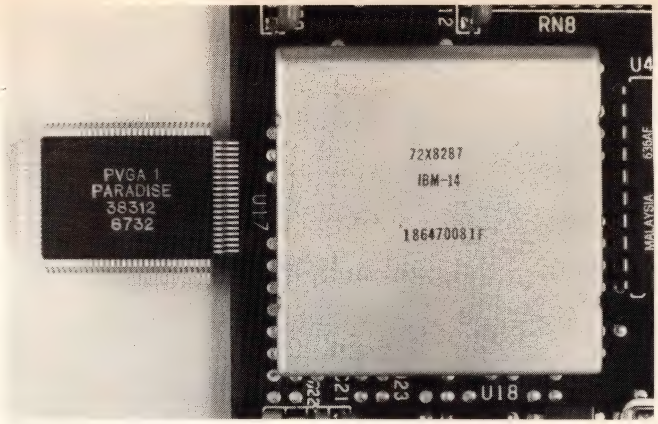

***Packing more features into a package that's 81% smaller** than IBM's VGA video controller, Paradise Systems' PVGA1 VGA chip lets you display 16 simultaneous colors at a resolution of 800×600 pixels. The chip also offers a 1024×768-pixel monochrome graphics resolution and increases processing performance because of its 16-bit architecture.*

standard 17 IBM VGA modes.

In case you already have a PS/2 Model 50, 60, or 80 and you long for higher resolution, you'll be relieved to know that you can order a graphics controller that will upgrade your PS/2's resolution to 1024×768 pixels. The Galaxy Mercury/2 board from GalaGraph Ltd also lets you select an 800×600-pixel mode. A special AutoCAD driver called MagniCAD provides windows that let you zoom in on any section of your design.

The board includes software drivers not only for AutoCAD but also for Ventura Publisher and Microsoft Windows. The board's Galaxy HI-PTK software package includes integration utilities and a library of graphics primitives and language bindings for various versions of Basic, C, Fortran, Pascal, and 8086/8088 assembler. This board provides 1M byte of display memory. You can buy this board for $2495 from the company's US distributor, Electrograph Sales Inc.

If budgetary considerations are your major problem, consider the $395 QuadVGA board from Quadram. Based on the 82C441/82A442 chip set from Chips and Technologies, the QuadVGA board provides register-level compatibility with IBM's VGA and comes with drivers for AutoCAD, Microsoft Windows, GEM, Lotus 1-2-3 and Symphony, and Ventura Publisher. The board has ports for both analog and digital monitors. **EDN**

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2. Hays, Dean and Bill Knapp, "Developing a VGA chip set with redefinable IC technology," *VLSI Systems Design*, November 1987, pg 68.
3. Williams, Tom, "VGA chips offer design opportunities and latest IBM compatibility," *Computer Design*, November 15, 1987, pg 50.

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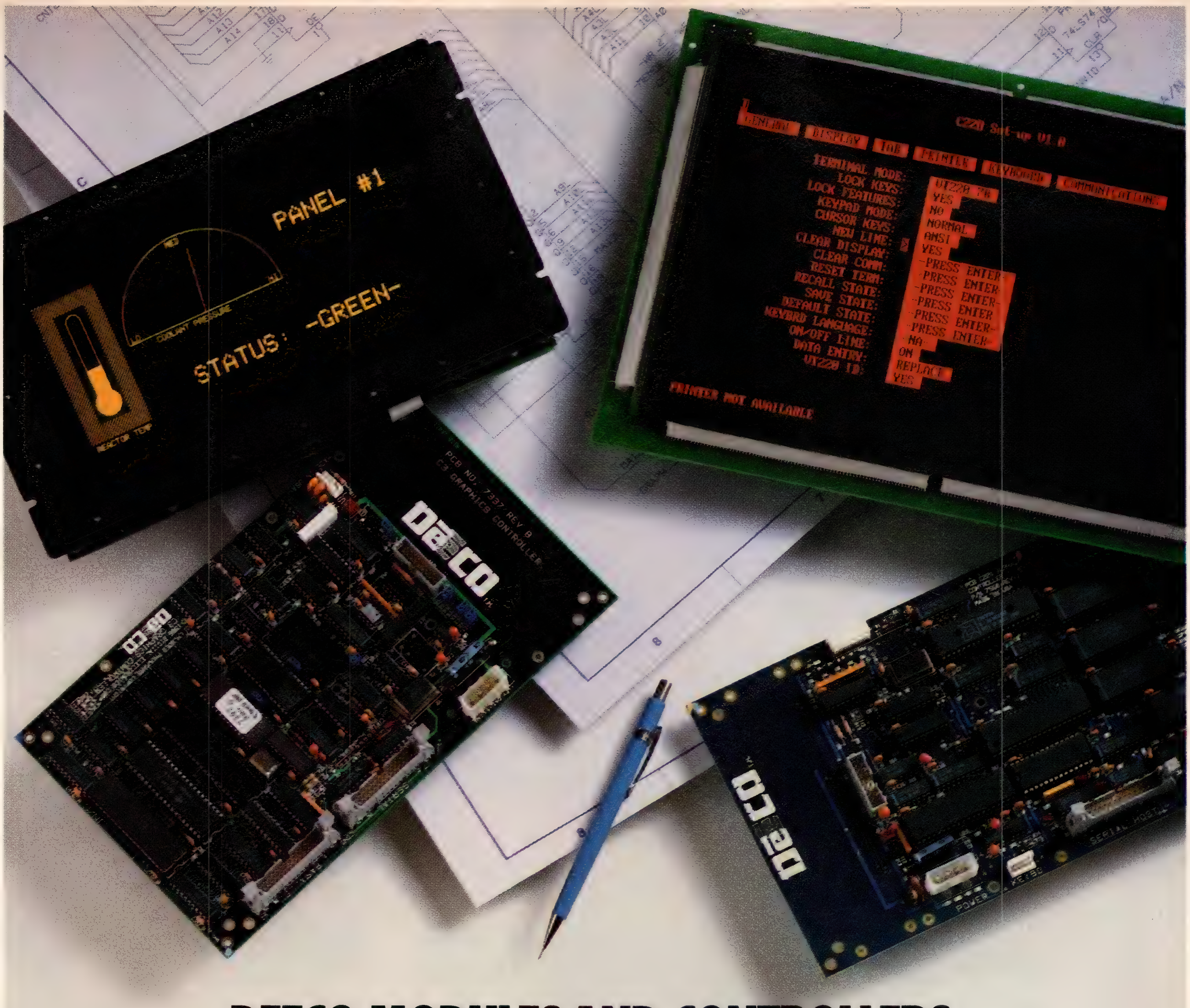

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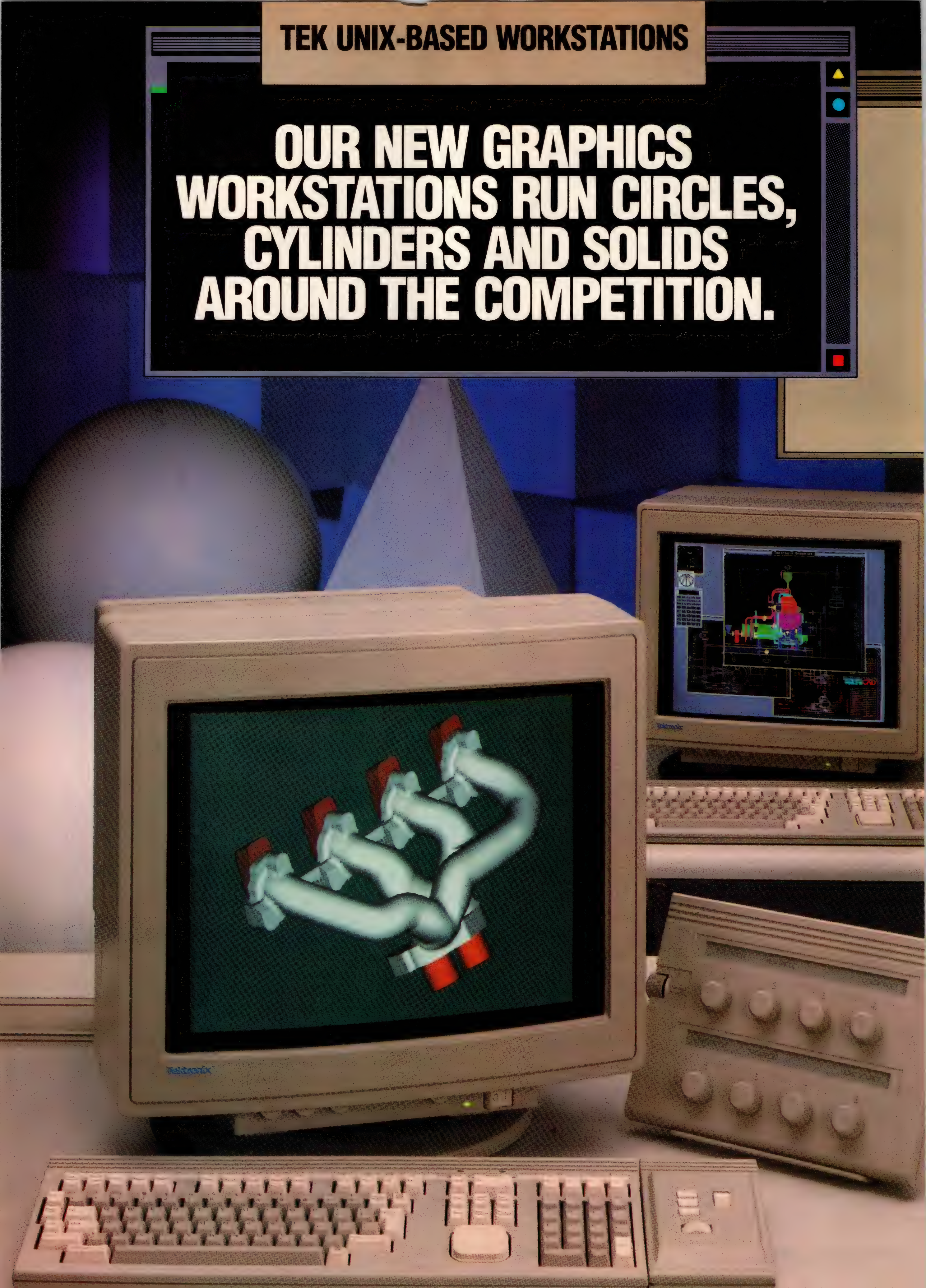
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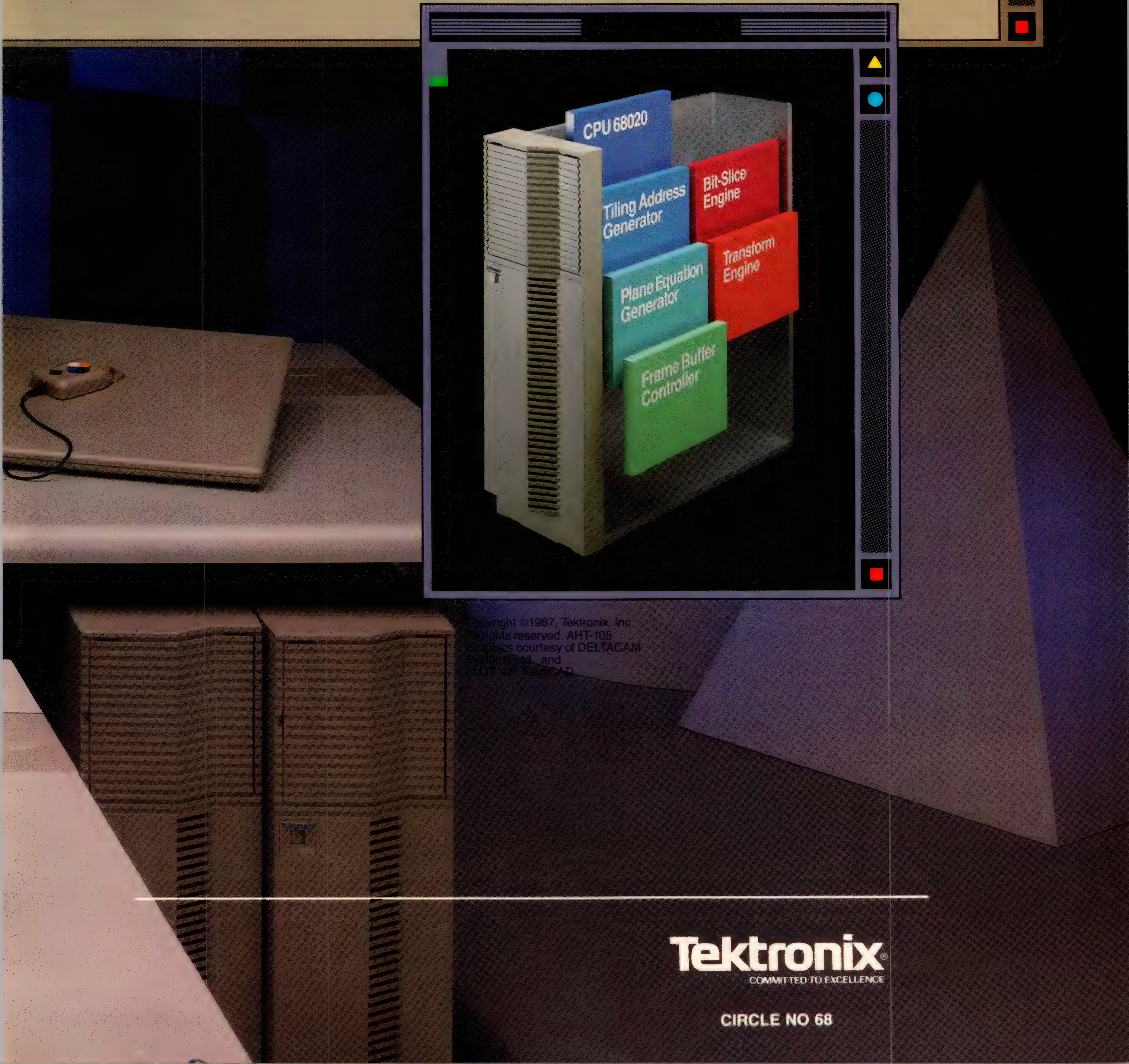

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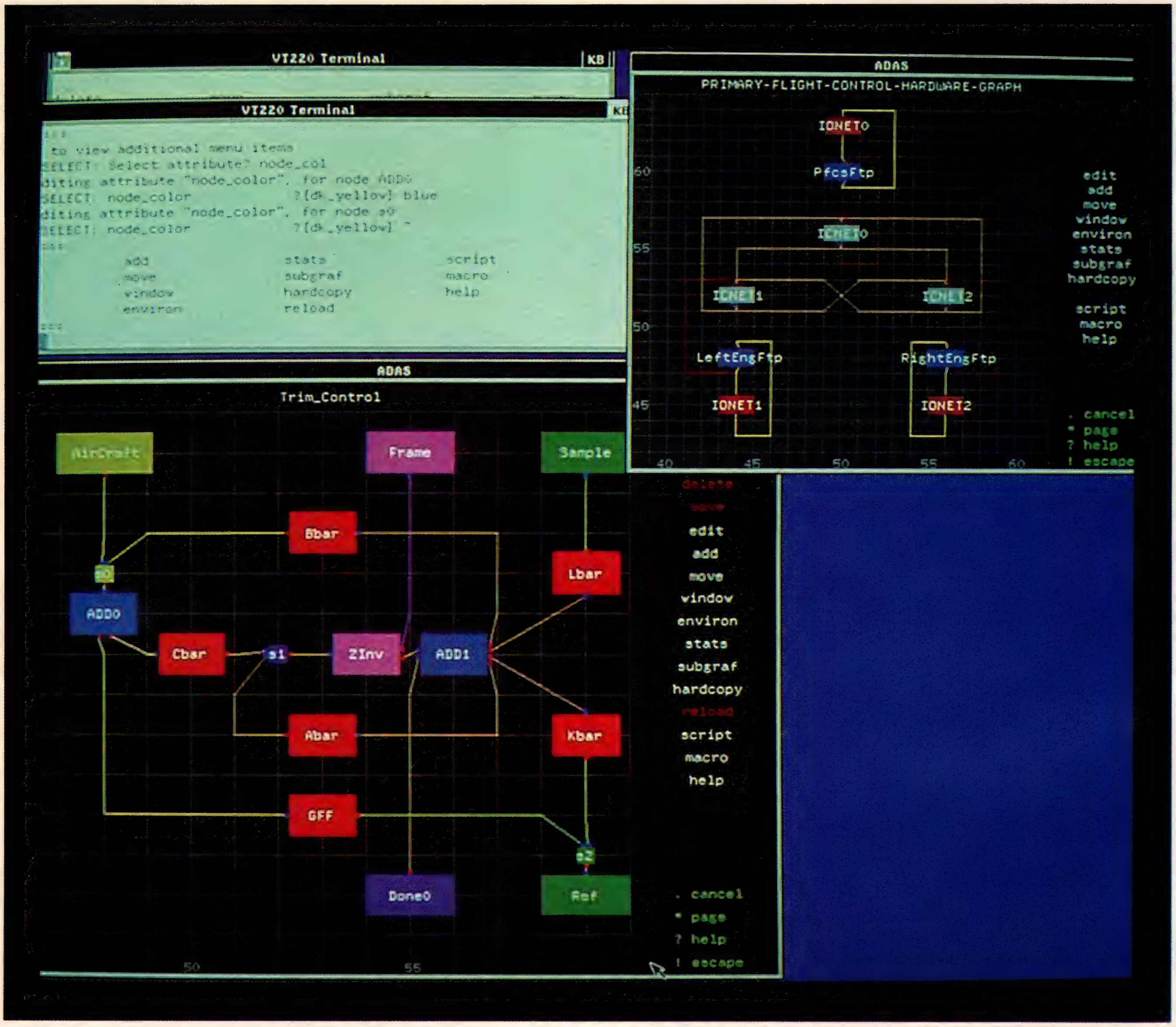

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ELECT: node_color              ?[dk_yellow] ~
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          move             subgraf           macro
          window           hardcopy          help
          environ          reload
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System-level CAE tools allow you to explore alternative system architectures *by simulating system performance with behavioral models of system components. This approach lets you ignore implementation details while dealing with architectural considerations at a very abstract level. (Photo courtesy Research Triangle Institute)*

PART TWO

DECADE 90

The future of system design

Developing CAE tools target top-down design of complex systems

The next decade's billion-transistor ICs will rapidly make manual system-design methods obsolete. If engineers are to tackle larger, more complex electronic designs, they will need automated design tools. Today's CAE tools help engineers develop system components. Tomorrow's tools will help designers develop entire systems.

Steven H Leibson, *Regional Editor*

The growing complexity of standard and custom ICs is making the task of designing electronic systems ever more arduous. Many vendors now offer CAE tools that help engineers manage such complexity, but today each tool handles, at best, only part of the job. These CAE products help you design ASICs or pc boards, or aid in the coding of software, for example, but no one product can yet help you do the total system design from top to bottom. Furthermore, today's automated IC-design tools can't transform inexperienced engineers into chip designers, and merely using a pc-board design system doesn't ensure that you'll come up with a good board design.

Over the next decade, however, CAE-tool vendors will start distilling design expertise into their tools so that inexperienced engineers can design noncritical parts of systems, and seasoned engineers can vastly improve their productivity. At the same time, system-level CAE tools will give designers better control over the definition and attainment of project goals.

Today's CAE tools work

Although most engineers still don't use CAE tools for any kind of design, a few designers are already using today's tools to create very complex systems. For example, Sequent Computer Systems (Portland, OR) used CAE tools from Mentor Graphics (Beaverton, OR) to develop two backplanes, three ASICs, and three pc boards for its Symmetry Series multiprocessor computers. The Symmetry computers are compatible with Sequent's earlier Balance Series.

Each Symmetry CPU board incorporates two processor subsections based on Intel (Santa Clara, CA) 80386 μPs. Sequent developed three ASICs for the Symmetry processor board: a 5000-gate cache-memory controller based on a gate array, a 10,000-gate bus-interface controller also based on a gate array, and a 14,000-gate data-path bus controller built with standard-cell technology. The company also used a 6000-gate serial-link-controller IC that it had designed for its earlier Balance Series computers. The company's engineers used Mentor Graphics tools to design all four of these ASICs.

Paul Gifford, manager of central systems engineering at Sequent, says the Mentor Graphics ASIC-design

Today's CAE tools are helping engineers design and simulate complex systems. *Engineers at Apollo Computer Inc used Mentor Graphics tools to develop the CPU board for the Apollo's DN4000 Series workstations.*

tools are "pretty robust" for developing chips at the 9000-gate level and are quite capable of developing ASICs having as many as 20,000 gates. Beyond that number of gates, he says, "the tools start to let go."

According to Gifford, Sequent also used Mentor Graphics tools to design the dual-processor boards for the Symmetry Series. Engineers performed simulations on about half of the processor board's circuitry, which is the equivalent of about 70,000 gates. A typical design iteration, including simulation, evaluation, and design editing, required about 24 hours.

Expanding the backplane

Sequent's engineers used MSpice analog simulation on the Mentor systems to help develop the Symmetry's backplane. They used bus-driver and -receiver models from the IC vendors and simulated several termination schemes to optimize the backplane's design. As a result, Symmetry's backplane has 26 slots. If the engineers hadn't been able to use analog simulation to verify the feasibility of the bigger backplane, says Walt Mayberry, Sequent's director of engineering, time-to-market pressures would have forced the company to use a more conservative 16-slot backplane, which would have limited the capacity of the machine.

Another computer manufacturer, Apollo Computer (Chelmsford, MA), also employed Mentor Graphics tools to design the processor board of one of its latest products, the DN4000 workstation. The DN4000's CPU board incorporates Motorola's (Phoenix, AZ) 68020 μP, 68881 floating-point coprocessor, and 68851 memory-management unit (MMU), plus other LSI components and 40 programmable-logic devices (PLDs).

Assorted device models

Apollo engineers used an assortment of device models to simulate the CPU board. They used hardware models for the 68020 and 68881, behavioral models for some of the other VLSI parts on the board, gate models for glue logic, and downloaded programs for PLDs and PROMs. Using this wide assortment of models, the designers were able to make design changes and perform simulations on the revised design in about 30 minutes.

Ted Elkind, a section manager in charge of Apollo's CAE logic-design tools group, estimates that the company saved one to two months of the 6-month prototyping cycle by using these CAE tools. Engineers brought the system debugger up on the CPU board in one day—for an earlier project, that task required about a week—and they had the operating system running on the new system in three weeks, instead of the usual three months.

Some shortcuts cost time

Apollo could have saved even more time by making better use of the simulation tools, Elkind notes. For example, because of time and resource constraints, Apollo didn't create hardware models of the 68851 MMU and the cache-tag comparator. Instead, the engineers wrote a simple, "pass-through" model of the MMU and a behavioral model of the cache-tag comparator.

When debugging the newly fabricated CPU board, the engineers spent a disproportionate amount of time finding and fixing design flaws centered around the MMU, and they discovered that the cache-tag comparator didn't operate according to its specifications. The comparator vendor had to redesign the part to meet the specifications and, fortunately, the revised part was ready in time for Apollo's first production run. Gifford says that better modeling of these two parts would have revealed these problems earlier in the design cycle and would have further reduced the time required to debug the new system.

Because of their experiences, both Sequent and Apollo strongly advocate the use of CAE development tools. Both companies intend to make even more use of simulation in future projects to further reduce debugging efforts and overall development time. However, the 24-hour design cycle required for the Sequent design shows that workstations can have a tough time coping with complex system design. In fact, most engineers would even consider the 30-minute time that Apollo achieved to be far too long.

Expert design assistance

These two examples illustrate the way that today's CAE tools can help engineers who have design expertise to create new designs more quickly. The CAE tools of the 1990s will go a step further: Just as general-purpose software, such as a spreadsheet, allows casual computer users to perform complex computational tasks without programming, the next decade's CAE tools will allow system-design engineers to create ICs without becoming IC designers.

Dr Prabhu Goel, president of Gateway Design Automation Corp (a Westford, MA, CAE-tool vendor) believes a dichotomy will emerge in IC-design CAE tools. He believes that some tools will mask the details of IC design so that inexpert chip designers can easily create noncritical portions of a chip. The critical portions of a chip—the ones that directly affect the IC's performance—will still be created by expert IC designers, who will use tools that allow for fine sculpturing of silicon, Goel says.

Artifical intelligence is already providing one way for engineers with some experience to become better IC designers. For example, NCR's (Fort Collins, CO) Design Advisor, an expert-system tool, can review IC designs and suggest improvements. The design rules built into the software were gathered from NCR's own IC engineering staff. The Design Advisor checks for several different types of design problems and can offer a wide range of advice concerning speed, testability, manufacturability, and silicon-area usage **(Fig 1).** To build the Design Advisor, NCR used the Proteus expert system developed by the MCC (Microelectronics and Computer Technology Corp) Artifical Intelligence Laboratory in Austin, TX.

But engineers use CAE software for more than just IC design. Some CAE tools aid in the development of pc boards or PLD programs. Unfortunately, the databases for these design tools are generally incompatible, creating an electronic Tower of Babel. One solution companies employ to overcome this mass of incompatible data is translation. For example, Aida Corp (Santa Clara, CA) offers software that performs file-format conversion, which allows Aida's system-design tools to accept design information from Mentor, Viewlogic, Tegas, and Hilo systems.

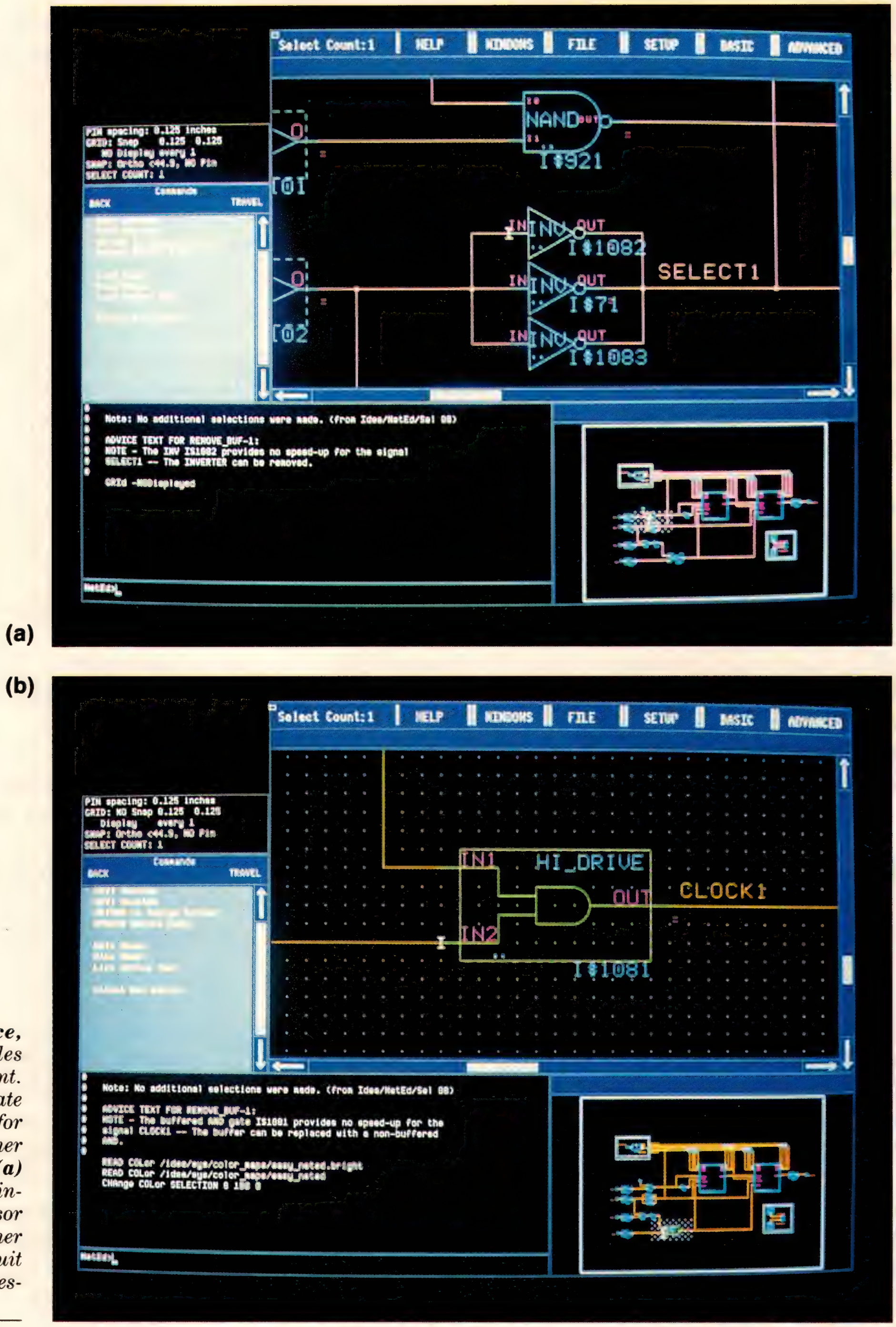
A standard language will allow for interchange

Translation is not the solution to the basic problem of incompatibility: If each CAE-tool vendor were to write translators for selected data-file formats, the industry would end up with an incomplete solution at a horrendous cost in development time. Instead of using translation, CAE-product vendors will employ standard interchange languages such as EDIF—the Electronic Design Interchange Format—to help eliminate database-format incompatibilities in the 1990s. EDIF allows CAE systems to exchange engineering information, and it encompasses several types of engineering documents or "views," including mask layouts, documents, behavioral descriptions of circuits, schematics, and net lists.

Some companies plan to take EDIF beyond hardware design. Cadre Technologies Inc (Providence, RI) has proposed a set of extensions to EDIF version 2 0 0 to accommodate software developed with CASE (computer-aided software engineering) tools. The EDIF Technical Committee, sponsored by the Electronic Industries Association (EIA) is currently considering that proposal.

EDIF allows CAE systems to exchange only low-level design information. Hardware definition languages

PART TWO
DECADE 90
The future of system design



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   NO Display every 1
SNAP: Ortho <44.9, NO Pin
SELECT COUNT: 1
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Note: No additional selections were made. (from Idea/NetEd/Sel 08)

ADVICE TEXT FOR REMOVE_BUF-1:
NOTE - The INV I$1082 provides no speed-up for the signal
SELECT1 -- The INVERTER can be removed.

GRId -NODisplayed
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NetEd>
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PIN spacing: 0.125 inches
GRID: NO Snap 0.125  0.125
   Display    every 1
SNAP: Ortho <44.9, NO Pin
SELECT COUNT: 1
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Note: No additional selections were made. (from Idea/NetEd/Sel 08)

ADVICE TEXT FOR REMOVE_BUF-1:
NOTE - The buffered AND gate I$1081 provides no speed-up for the
signal CLOCK1 -- The buffer can be replaced with a non-buffered
AND.

READ COLor /idea/sys/color_maps/easy_neted.bright
READ COLor /idea/sys/color_maps/easy_neted
CHAnge COLor SELECTION 0 100 0
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NetEd>
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Fig 1—Based on artificial intelligence, *NCR's Design Advisor CAE tool provides expert design assistance for IC development. The program uses several criteria to evaluate IC designs, and it also gives advice. Here, for example, it recommended that the designer eliminate one of three parallel inverters* ***(a)*** *and suggested the use of an unbuffered instead of a buffered gate* ***(b).*** *Design Advisor made both suggestions because the designer selected components that don't speed circuit operation yet use more silicon than necessary.*

(HDLs), however, promise to allow designers to manage and exchange information at several levels of abstraction, from the system level down. Engineers will need system-level CAE tools such as HDLs to help them design systems around billion-transistor ICs. System development of that complexity demands a structured approach such as that supplied by HDLs.

A few HDLs already exist; they include Gateway's Verilog-XL, Aida's ADL, VHDL (the VHSIC hardware definition language developed for the Department of

Defense's VHSIC (very-high-speed IC) program), and ISP′ from Endot (Cleveland, OH). Verilog-XL and ISP′ incorporate a syntax resembling the C software programming language. VHDL uses an Ada-like syntax.

According to Dr Thomas A Zimmerman, director of VHSIC programs at TRW's Electronics and Technology Div, VHDL's current lack of a good simulator is a major shortcoming of the language. Dr Zimmerman feels that HDLs will be extremely important for communicating the specifications and requirements of systems and system components. In fact, he says, in much the same way that Ada has become the software language of choice for military systems, VHDL may become mandatory for systems commissioned by the Department of Defense.

Intermetrics Inc (Cambridge, MA) developed the existing VHDL tool set under a VHSIC contract. In December 1987, a revised version of VHDL became IEEE standard 1076. Intermetrics plans to introduce software during 1988 that supports this IEEE standard; the software will include an analyzer that's somewhat like an HDL compiler, as well as a reverse analyzer, and both interactive and batch simulators. Intermetrics also plans to support other CAE vendors who wish to develop VHDL tools—the company will share its front-end software technology with them.

HDLs support many levels

HDLs allow you to describe circuits at the gate, functional, and behavioral levels. For top-down designs, you can use an abstract, behavioral description that avoids the clutter of implementation details and enables you to focus on how the circuit performs. Later, you can design the detailed circuit by using the HDL's lower-level syntax.

Because HDLs give you the ability to describe a system component behaviorally, you can simulate a complex system before designing the circuitry. For example, Gateway's Verilog-XL includes a mixed-mode simulator that accepts behavioral, functional, and gate-level models simultaneously. According to Dr Goel, hardware designers working for some of Gateway's clients have become software gurus while learning to define systems by using Verilog.

One of the benefits of HDL-based hardware design, says Goel, is that it permits the easier partitioning of large designs into blocks that one person can handle. Goel also believes that HDLs help move much of the design process to the conceptual level, freeing engineers from design details that frequently bog them down.

Other CAE experts, however, do not believe that today's hardware engineers will quickly abandon the design techniques they use today. Schematic circuit representations are firmly embedded in most engineers' work habits, and system-design tools that support those familiar ways are also appearing. Further, several CAE-tool vendors allow you to mix schematic and HDL representations. You should expect to use each design technique where it fits best. As usual, most engineers will adopt the available tools in ways that suit them, not the tool designers.

Graphic system design

An example of a system-level, graphic design tool is the ADAS (architecture design and assessment system) CAE tool set developed by the Research Triangle Institute (RTI, Research Triangle Park, NC). ADAS allows you to develop schematic representations of system data-flow and hardware configurations. Petri net simulators and analyzers then verify your design and simulate your system's performance. By using various definitions to map the execution of abstract operations onto system hardware resources, you can experiment with different levels of parallelism to find the optimum combination of hardware and software.

Honeywell (Minneapolis, MN) used ADAS to optimize the design of a video-image processor that will be used on NASA's space station. Honeywell simulated systems employing different network topologies (1-, 2-, and 3-bus systems, hypercube, and both unidirectional and bidirectional braided rings), different numbers of processors (four, eight, and 16), different processor speeds (2, 5, and 10 MIPS), and different bandwidths for interprocessor communications (2M, 5M, and 10M bytes/sec).

Honeywell used ADAS to simulate systems built with these various attributes. The company then decided that the optimum system configuration would have sixteen 10-MIPS processors that communicated over a dual bus at 5M bytes/sec. Clearly, system-level design tools such as ADAS allow you to make informed architectural decisions for very complex systems.

Getting chips from system tools

ADAS is strictly a system-level design tool, however. It produces descriptions of system components, but it doesn't help you design those components. You must

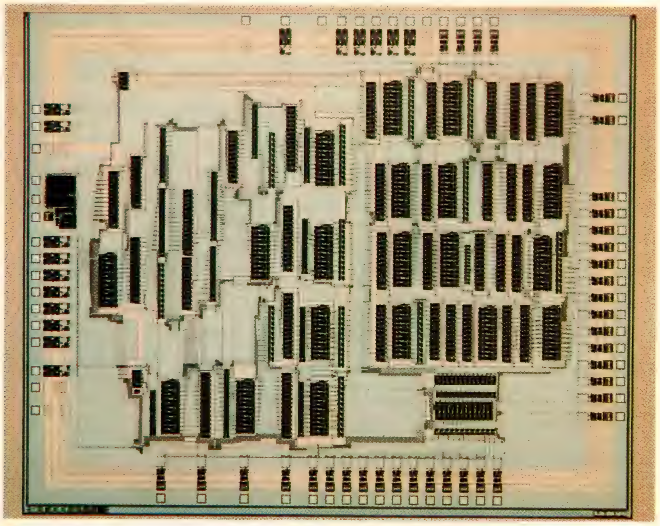

*Fig 2—**To develop the architecture for this edge-detection image-processor IC,** engineers at the Research Triangle Institute (RTI) used ADAS, RTI's system-level CAE tool. To create the IC, they then transferred the architectural design to Silicon Compiler Systems' Genesil silicon compiler. In the future, standard hardware definition languages such as VHDL will make the conversion process automatic.*

use other CAE tools for the individual component designs. For example, RTI recently created a system definition of an optical processor that employs the Sobel algorithm for edge detection. After using ADAS to create, simulate, and verify a system architecture, the RTI engineers transferred the architecture to Silicon Compiler Systems Corp's (San Jose, CA) Genesil compiler and implemented the various functional blocks in the optical processor (registers, multiplexers, adders, etc) with elements from the Genesil library. They then used Genesil to simulate the compiled version of the image processor as part of the verification process.

In an additional verification step, the engineers created a VHDL description of the edge-detection chip and verified the design with a VHDL simulator. Of course, the working chip provided the ultimate verification of the design (**Fig 2**). In the future, tools such as ADAS and Genesil will exchange design information directly, using automatically generated VHDL files. Both RTI and Silicon Compiler Systems are currently working on VHDL interfaces for their CAE tools.

Bearing the cost

Although CAE tools such as those mentioned here clearly boost engineering productivity, it's not clear how many companies will bear the cost of these tools. Most CAE tools run on workstations that cost at least $10,000. Add to this several thousand dollars—or tens of thousands of dollars—for the software, and you arrive at a total outlay that represents a substantial investment per design engineer.

Companies that believe that a shortened development cycle and optimized designs justify such a large outlay are already adopting these tools. If you're waiting for the tools to get a bit better before you adopt them, consider that at any point in time, CAE tools will always seem inadequate for the task of designing leading-edge systems. However, engineers routinely push their tools beyond commonly accepted limits to design state-of-the-art systems, and semiconductor technology shows no signs of slowing down to wait for the CAE tools to catch up.

From the Sequent and Apollo success stories, you can see that engineers at some firms have taken the sometimes difficult measures necessary to master today's design tools, and are already making plans to use tomorrow's offerings. Companies that cannot or will not invest in CAE tools may find themselves less able to tackle the large projects that will become more common in the next decade. Such companies will find themselves at a competitive disadvantage in the 1990s. **EDN**

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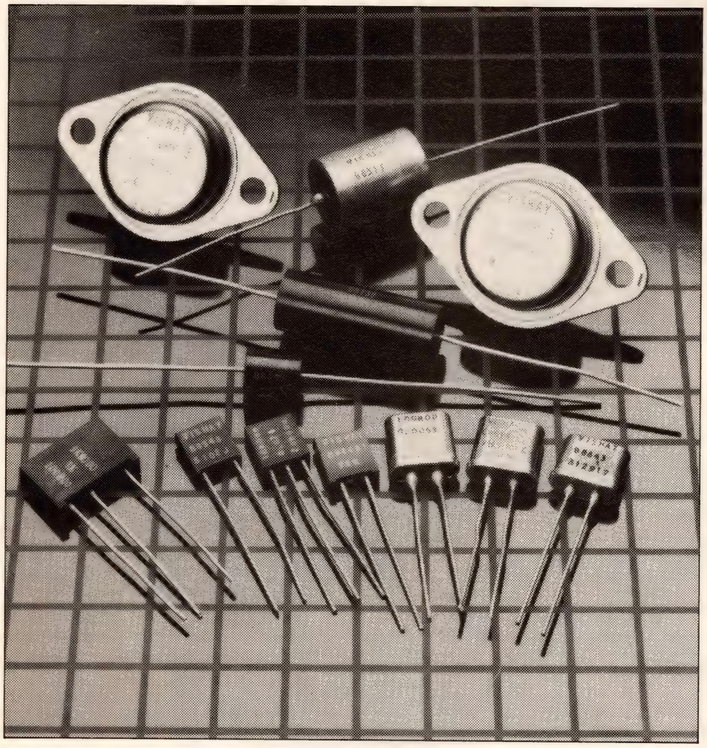

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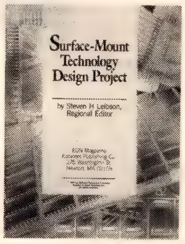
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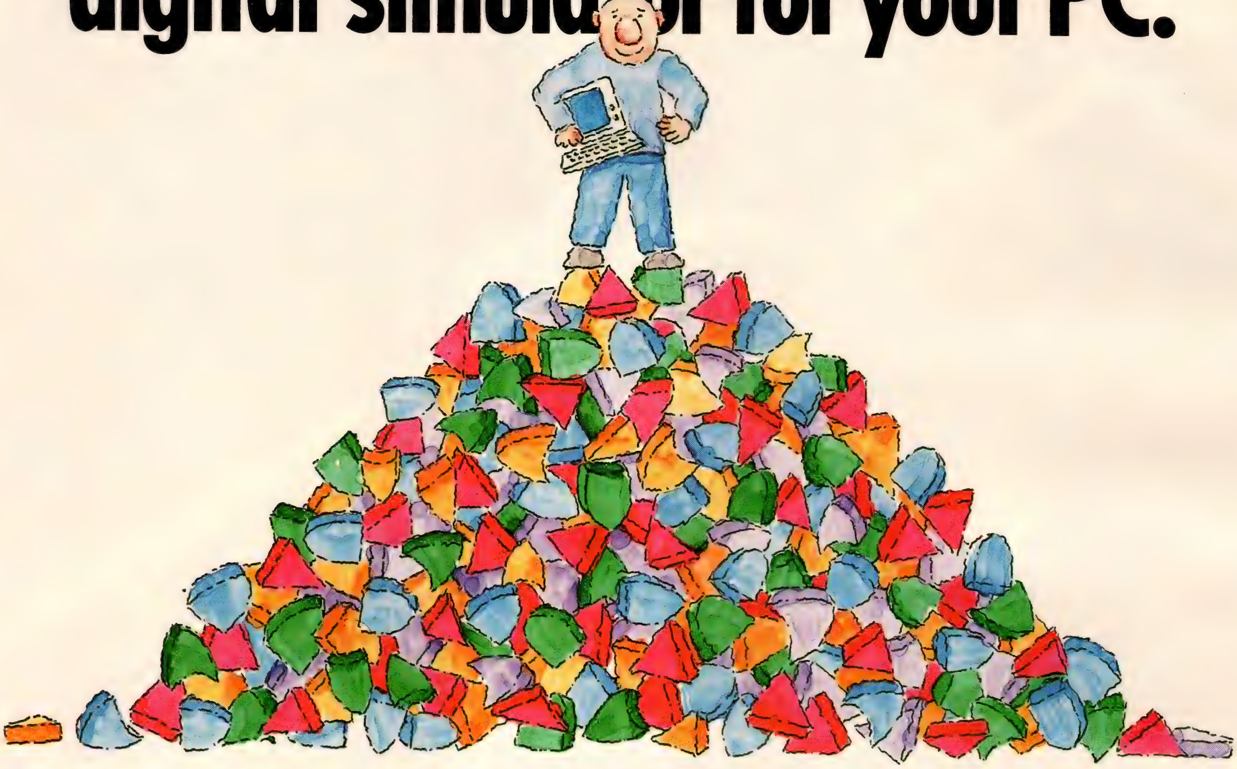

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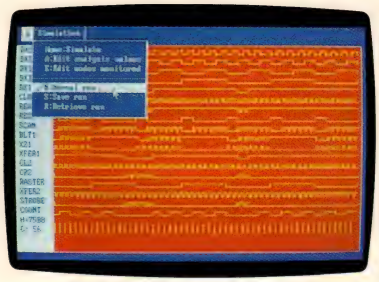

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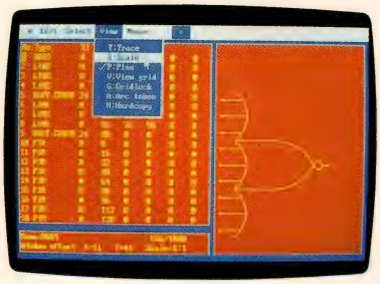

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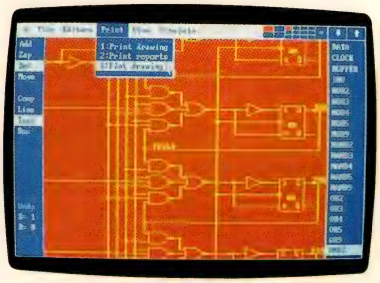

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CIRCLE NO 73

Design method yields low-noise, wide-range crystal oscillators

A characterization technique allows you to design frequency-determining networks for tunable crystal oscillators. The method yields oscillators that provide a wide tuning range and exhibit low-noise performance. The design methodology accurately quantifies all effects relevant to oscillator performance.

Tim L Hillstrom, *Hewlett-Packard Co*

Traditionally, designing crystal oscillators that have wide tuning range and acceptable noise performance requires time-consuming trial-and-error methods. However, you can use a straightforward design procedure to achieve a tuning range of hundreds of ppm without compromising noise performance. By characterizing the tuning range of the frequency-determining network of a crystal oscillator, you can accurately quantify all the effects that determine oscillator performance and fully include them in your design.

This design technique extends the traditional approach that uses a crystal's equivalent-circuit model—a model that fails to adequately characterize the crystal in difficult designs. The equivalent-circuit approach simply does not accommodate such relevant effects as off-resonance lossiness, crystal-model element variation with frequency, and spurious modes. Traditionally, these effects are lumped into a vague term called "crystal pullability."

The material given here will concentrate on feedback-type oscillators using crystals configured in the series-resonant mode **(Fig 1a)**. Note, however, that the design techniques presented here are applicable to other topologies as well. In this block diagram, H(f) is a low-Q bandpass filter that selects the desired harmonic. G_2 is a buffer that provides a low-impedance termination for the frequency-determining network, and G_1 is a nonlinear gain block that provides the variable gain or amplitude limiting necessary for stable oscillation. The gain of G_1 decreases monotonically as a function of signal level. When the circuit turns on (and signal levels are low), G_1 varies to provide an open-loop gain greater than three to ensure that the circuit oscillates. Once the circuit is oscillating and signal levels attain a steady-state condition, G_1's gain is approximately unity.

The frequency-determining network contains the crystal and associated tuning elements. This circuit block is a 1-port network ideally described as $Z_f(f)$. For optimum performance, you must minimize undesirable admittances, such as those attributable to stray capacitance and varactor-isolating resistors. The dotted ground connection (which carries negligible current) from the frequency-determining network is an example of a low-admittance stray network path.

In order for the circuit to oscillate, open-loop phase

The equivalent-circuit approach to designing crystal oscillators simply does not accommodate a number of relevant effects.

shift must equal 0°. Because the circuit in **Fig 1** contains two frequency-dependent blocks, a number of harmonic-selecting filter and frequency-determining-network phase combinations will provide an overall loop phase shift of 0°. For two reasons (maximum loop gain and minimum phase noise), it's best to have 0° phase shift in each network. The design method shown here uses 0° phase shift as a condition.

Now it's time to concentrate on the crystal loop—the closed path around R_{t1}, the frequency-determining network, and R_{t2}. The crystal loop partially determines the oscillator's phase noise and totally determines the frequency tuning. The frequency-determining aspect of the loop is true because everything outside the crystal loop is independent of frequency over the narrow frequency range of interest. In the model, G_1's input impedance is infinite, and G_2's output impedance equals zero. If I_{STRAY} is negligible, you can consider the frequency-determining network to be a 1-port impedance $Z_f(f)$. Therefore, the relevant equations for oscillation and noise become

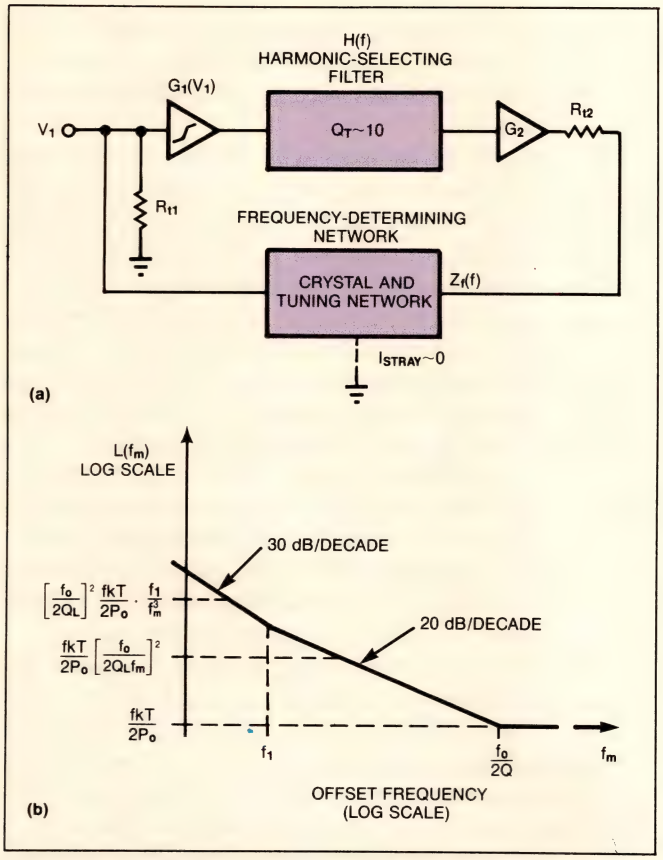
H(f)
HARMONIC-SELECTING FILTER
$G_1(V_1)$
V_1
Q_T~10
G_2
R_{t2}
R_{t1}
FREQUENCY-DETERMINING NETWORK
CRYSTAL AND TUNING NETWORK
$Z_f(f)$
I_{STRAY}~0
(a)
$L(f_m)$
LOG SCALE
30 dB/DECADE
20 dB/DECADE
$\left[\frac{f_o}{2Q_L}\right]^2 \frac{fkT}{2P_o} \cdot \frac{f_1}{f_m^3}$
$\frac{fkT}{2P_o}\left[\frac{f_o}{2Q_L f_m}\right]^2$
$\frac{fkT}{2P_o}$
f_1
$\frac{f_o}{2Q}$
f_m
OFFSET FREQUENCY
(LOG SCALE)
(b)

Fig 1—Because this circuit includes two frequency-dependent blocks, *a number of harmonic-selecting filter and frequency-determining-network phase combinations will provide an overall loop phase shift of 0°—a necessary condition for oscillation.*

$$I_m\,[Z_f(f)] = 0 \tag{1}$$

$$Q_L(f) = \frac{f_o}{2(R_{t1} + R_{t2} + \mathrm{Re}[Zf(f)]} \cdot \frac{d\mathrm{Im}[Zf(f)]}{df}, \tag{2}$$

where $Q_L(f)$ is the Q of the frequency-determining network. This parameter is also known as the "loaded Q" of the crystal. The dominant parameter under designer control, $Q_L(f)$, determines the oscillator's noise level. According to Leason's equation, the single-sided phase noise equals

$$\begin{aligned} L(f_m) &= \frac{FkT}{2P_o}\left[1 + \left(\frac{f_o}{f_m 2Q_L}\right)^2\right]\left[1 + \frac{f_1}{f_m}\right] \qquad (3)\\ &\cong \frac{FkT}{2P_o}\left[\frac{f_o}{f_m 2Q_L}\right]^2 \text{ for } f_1 < f_m < \frac{f_o}{2Q_L}\\ &\cong \frac{FkT}{2P_o}\left[\frac{f_o}{2Q_L}\right]^2\left[\frac{f_1}{f_m^3}\right] \text{ for } f_m < f_1 < \frac{f_o}{2Q_L}, \end{aligned}$$

where

f_0=oscillation frequency

$f_m \approx f - f_0$=offset frequency

f_1=[1/f] noise corner ($<f_0/2Q_L$)=resonator half bandwidth

k_T=thermal noise floor=−174 dBm/Hz

F=noise figure of the circuit

P_0=output power

Q_L=loaded Q

Fig 1b illustrates this phase-noise characteristic. It's worth noting that the crystal itself can contribute noise that exceeds that predicted by Leason's equation. This noise is generally attributable to contaminants in the crystal. Proper crystal-manufacturing techniques (in a clean room) and cold- or resistive-weld sealing techniques minimize the problem.

Inspection of **Eq 2** and **Eq 3** suggests that for minimum phase noise over the entire tuning range, $Z_f(f)$ must have an imaginary part having a large slope and a real part that remains small. Ideally, oscillator loop gain remains constant over the tuning range. This condition ensures oscillator start-up and minimal AM noise over the tuning range. You can realize constant loop gain by selecting $Z_f(f)$ such that it has a small and fairly constant real part over the tuning range. A constant Q_L is also desirable because it provides consistent noise performance over the tuning range and also simplifies the design of the tuning network. For constant loop gain and optimal noise performance over the tuning range, therefore, you'll need a $Z_f(f)$ that has a large slope, an imaginary part that's fairly linear, and a real part that's small and fairly constant.

You must observe one final requirement for stable oscillation—the imaginary part of $Z_f(f)$ must equal zero at only one frequency over the entire frequency range in which sufficient loop gain exists for oscillation. To meet this requirement, you'll need a crystal that has a monotonic reactance-vs-frequency characteristic.

Frequency-determining network

To attack the design problem, first consider an ideal ($C_0=0$) crystal connected in series with a variable tuning capacitor **(Fig 2).** As **Fig 2** illustrates, this network meets all the requirements stated above. The variable tuning capacitance C_S shifts the crystal reactance down by a variable amount that's essentially independent of frequency over a small fractional frequency range. Oscillation occurs at the point where the shifted reactance curve crosses zero. A straightforward analysis yields the equation

$$\frac{\Delta f}{f_0} = \frac{C_m}{2C_{smin}}\left[1 - \frac{1}{C_R}\right], \qquad (4)$$

where Δf is the tuning range and C_R is the tuning-capacitance ratio (C_{smax}/C_{smin}).

Clearly, a series tuning capacitor can only shift the oscillation frequency to a value above the series-resonant frequency of the crystal. Therefore, most VCXOs (voltage-controlled crystal oscillators) using this configuration are tuneable to a frequency above the series-resonant frequency of their crystals. You can lower the tuning frequency by adding an inductor in series with the tuning capacitor. Although adding inductance helps avoid the spurious modes that typically occur at frequencies above the crystal's series-resonant frequency, the addition introduces susceptibility to magnetic-pickup problems.

Now consider a network **(Fig 3)** in which the ideal crystal's C_0 is greater than 0 pF. Clearly, this circuit fails to meet two of the previously cited requirements—the real part of Z_X is not constantly low, and the imaginary part is not linear. You can remove the effects of C_0 by adding an appropriate inductor L_0 to form a parallel-resonant circuit. Unfortunately, you cannot select L_0's value based on measured or specified values of C_0, because the crystal model is not adequate for difficult applications.

The best design approach is to measure $Re[Z_X(f)]$ and $Im[Z_X(f)]$ over the entire tuning range. You then mathematically (or physically) add enough parallel inductance to satisfy the design requirements. Although in theory it's possible to precisely meet the crystal's requirements, the crystal could deviate substantially from any modeled performance in practice. However, the approach does allow you to quickly evaluate crystal prototypes in environments that mirror the actual application. This advantage can be a real time saver.

To get down to specifics, let's design an 80-MHz

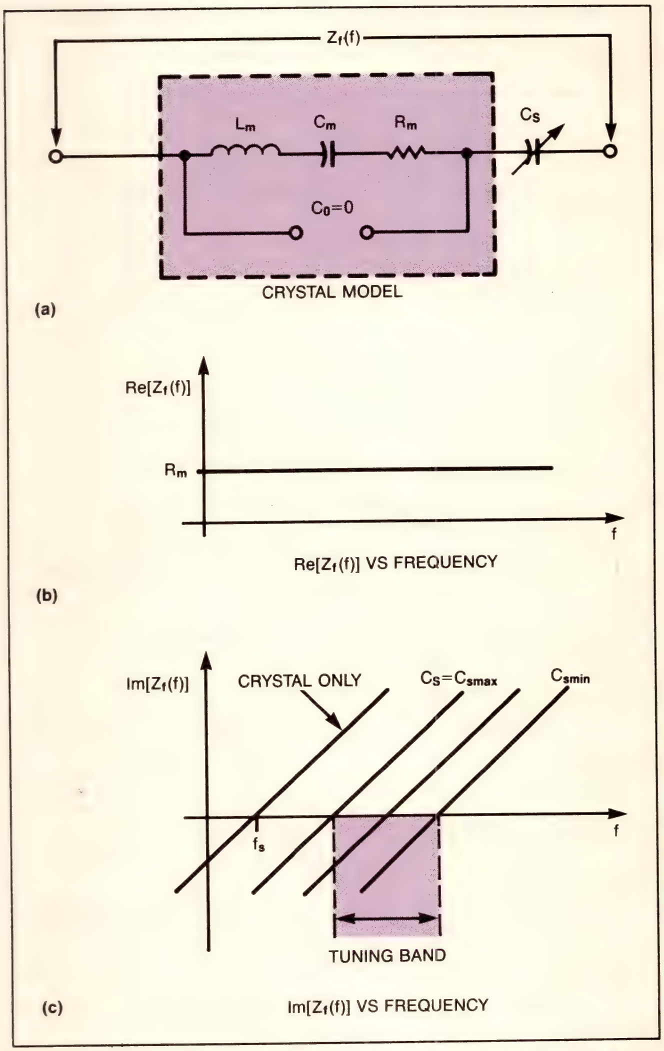

*Fig 2—**Because a series tuning capacitor can only raise the oscillation frequency** above the series-resonant frequency of the crystal, oscillators using this configuration are tunable to frequencies above their crystal's series-resonant frequency.*

Proper crystal-manufacturing techniques and cold- or resistive-weld sealing techniques can minimize intrinsic crystal noise problems.

VCXO for use in a phase-locked loop that must accommodate a ±15-ppm absolute error in its reference frequency. Typically, low-cost crystals specify a ±5-ppm absolute frequency error, a ±15-ppm aging error over 10 years, and a ±10-ppm variation as a function of temperature (over an industrial operating range). To accommodate all these error sources, the oscillator must have a ±45-ppm tuning-range capability —that is, $\Delta f=90$ ppm. This is considered a very wide tuning range for a low-noise, 80-MHz VCXO.

In some cases, you could use two devices to develop the required overall tuning capacitance—a mechanical trimmer capacitor for crystal-frequency error and aging, and a varactor to satisfy the remaining tuning requirement. In this example, however, the design will use a varactor for the entire 90-ppm tuning range. **Eq 4** shows that a wide tuning range requires a large varactor capacitance ratio (C_R), a small C_{smin}, and an appropriately large crystal motional capacitance C_M. Increasing C_M may decrease the unloaded-crystal Q, so you must make some tradeoffs to realize the optimum combination.

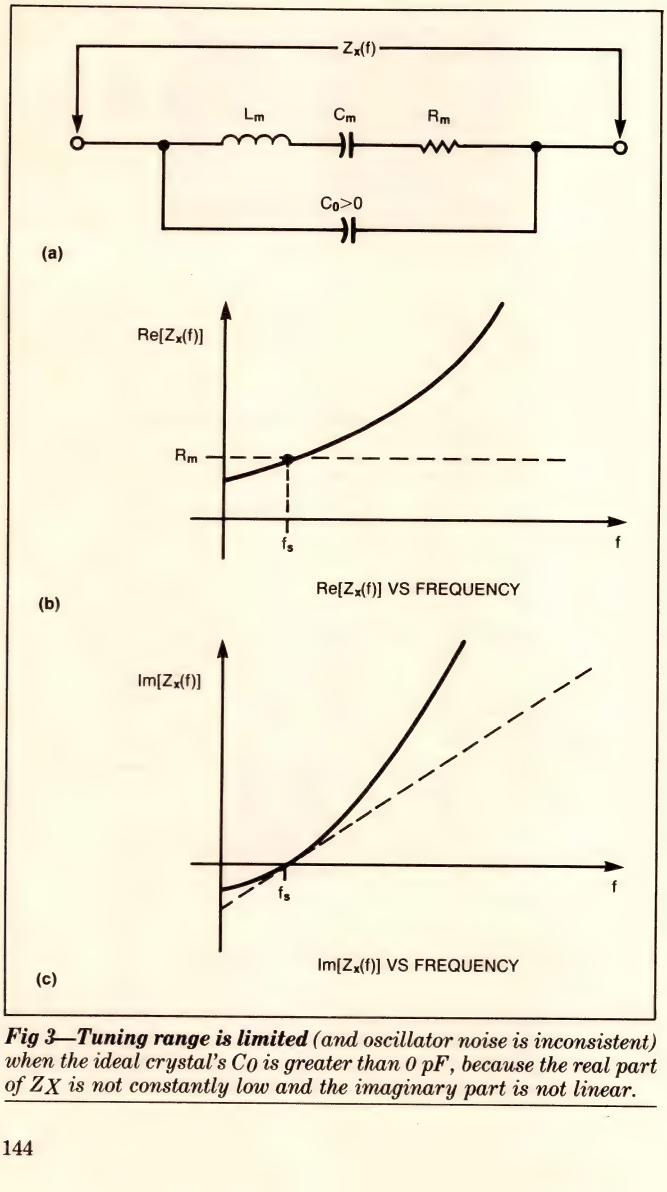

***Fig 3—Tuning range is limited** (and oscillator noise is inconsistent) when the ideal crystal's C_0 is greater than 0 pF, because the real part of Z_X is not constantly low and the imaginary part is not linear.*

To obtain a large varactor C_R, you must use a hyper-abrupt diode. For a hyper-abrupt VHF varactor like the BB105, $C_R \approx 5.5$ and $C_{smin}=2.2$ pF. From **Eq 4**, therefore, C_M must be at least 0.5 fF to ensure $\Delta=90$ ppm. The mean frequency (80 MHz by design in this case) over the tuning range is

$$\bar{f} = f_o\left[1 + \frac{C_m}{4C_{smin}}\left(1 + \frac{1}{C_r}\right)\right]. \qquad (5)$$

From **Eq 5**, the crystal's series-resonant frequency comes out to 79.99462 MHz, or 67 ppm below 80 MHz. The crystal must have no spurious modes or aberrant characteristics over the tuning range—between 22 and 112 ppm above the series resonant frequency.

This design is based on the properties of an ideal crystal. In a real-world situation, you'll have to measure a real crystal to determine the tuning-band measurements of the frequency-determining network. You then use this data to select the correct varactor and a crystal with the proper frequency.

To add detail to the theory, **Fig 4** illustrates a 2-transistor feedback oscillator that effectively implements the block diagram of **Fig 1.** L_1, C_1, and C_2 combine to set the desired crystal harmonic frequency. D_1, which is isolated from the crystal, provides amplitude limiting. D_1's impedance decreases with signal level. This impedance drop reduces Q_1's voltage gain and thereby implements the G_1 variable-gain block of **Fig 1.** The network comprising the crystal, L_2, and D_2 determines the oscillator's frequency. Q_2 isolates the tank from the crystal and provides a low-impedance termination for the crystal's closed loop, composed of R_{t1}, the crystal, D_2, and R_{t2}. Q_1 supplies the voltage gain necessary for oscillation and also provides a low-impedance termination for the crystal loop.

To start, you must adjust the oscillator's frequency-determining network to run at 0° phase. To do this, you can substitute an ac-coupled resistor whose value is equal to the typical value of $\mathrm{Re}[Z_f(f)]$ over the tuning range. You then select C_1 and/or C_2 to establish the oscillator's desired operating frequency—80 MHz in this case. You then replace the resistor by the frequen-

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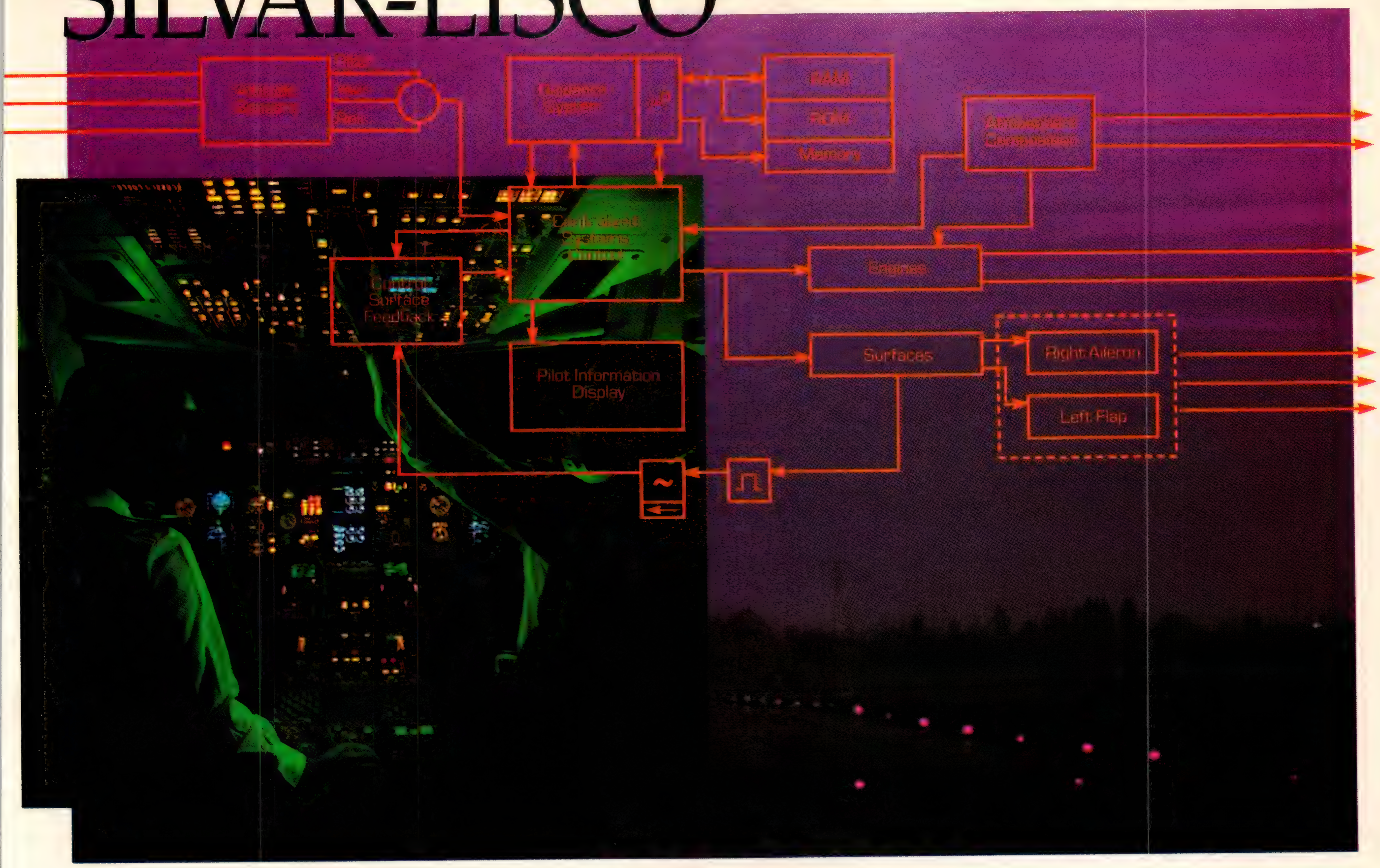

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CIRCLE NO 74

It's hard to precisely meet theoretical crystal requirements because the crystal may deviate substantially from any modeled performance in practice.

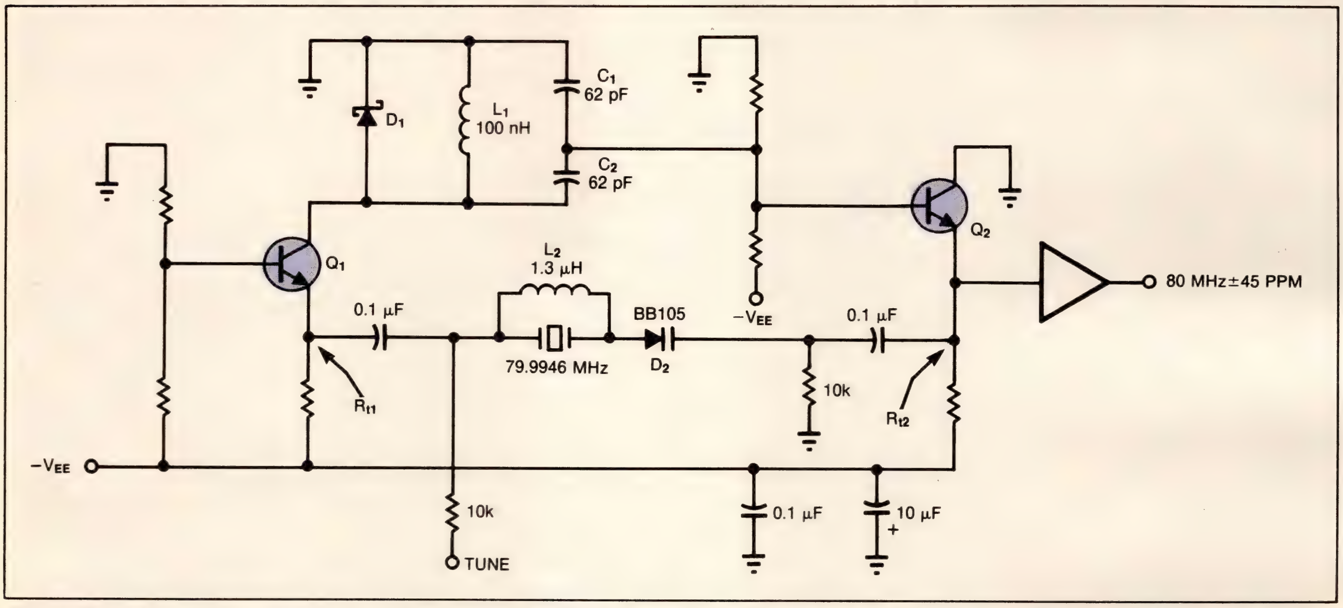


Fig 4—C1, C2, and L1 combine to set the desired crystal harmonic frequency *in this 2-transistor feedback oscillator. The network comprising the crystal, L2, and D2 determines the oscillator frequency.*

cy-determining network to complete the design.

When you physically add the frequency-determining network, you should minimize stray admittances. You can do this by removing the ground plane from beneath the frequency-determining network and using large impedance values for the varactor's bias resistors. Note that some nodal impedances in the frequency-determining network are very high—900Ω in this case. To maintain this high impedance at high frequencies, pay strict attention to the physical layout. At this point, the oscillator's tuning range should be very close to the design goal. In addition, noise performance will be fairly constant over the tuning range.

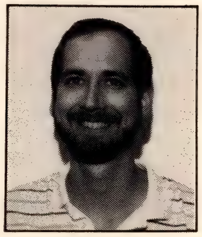
Several mechanisms will act to limit your attempts to achieve greater and greater oscillator tuning ranges. Spurious operating modes are inevitable as you attempt to tune further away from the crystal's series-resonant frequency. Other crystal characteristics can also cause problems.

Crystal reactance, for example, may become nonmonotonic with frequency and thus cause unstable tuning. Maintaining high impedance at high frequencies is another problem area. The crystal's high-impedance node has a design impedance of

$$Z(f) \cong R_{t1} + R_m + j\frac{f - f_5}{\pi f_o^2 C_m}.$$

Stray capacitance and the varactor-bias ports will eventually limit your attempts to increase the design impedance. In addition, the accuracy of measurements of the frequency-determining network decreases as you attempt to develop very high impedance levels. For example, if you use an HP3577A vector network analyzer and an HP35677A s-parameter test set, the measurements will have adequate accuracy for impedances between 0.5 and 1000Ω. **EDN**

Author's biography



Tim Hillstrom is a design engineer at the Hewlett-Packard Lake Stevens Instrument Div (Everett, WA), where he is responsible for designing RF circuits for frequency-domain instruments. A 5-year employee at HP, Tim holds a BSEE degree from the University of Portland and an MSEE from the University of Washington. In his spare time, Tim enjoys music; he plays the piano and the guitar. He also enjoys playing basketball and is a tennis fanatic.

Article Interest Quotient (Circle One)
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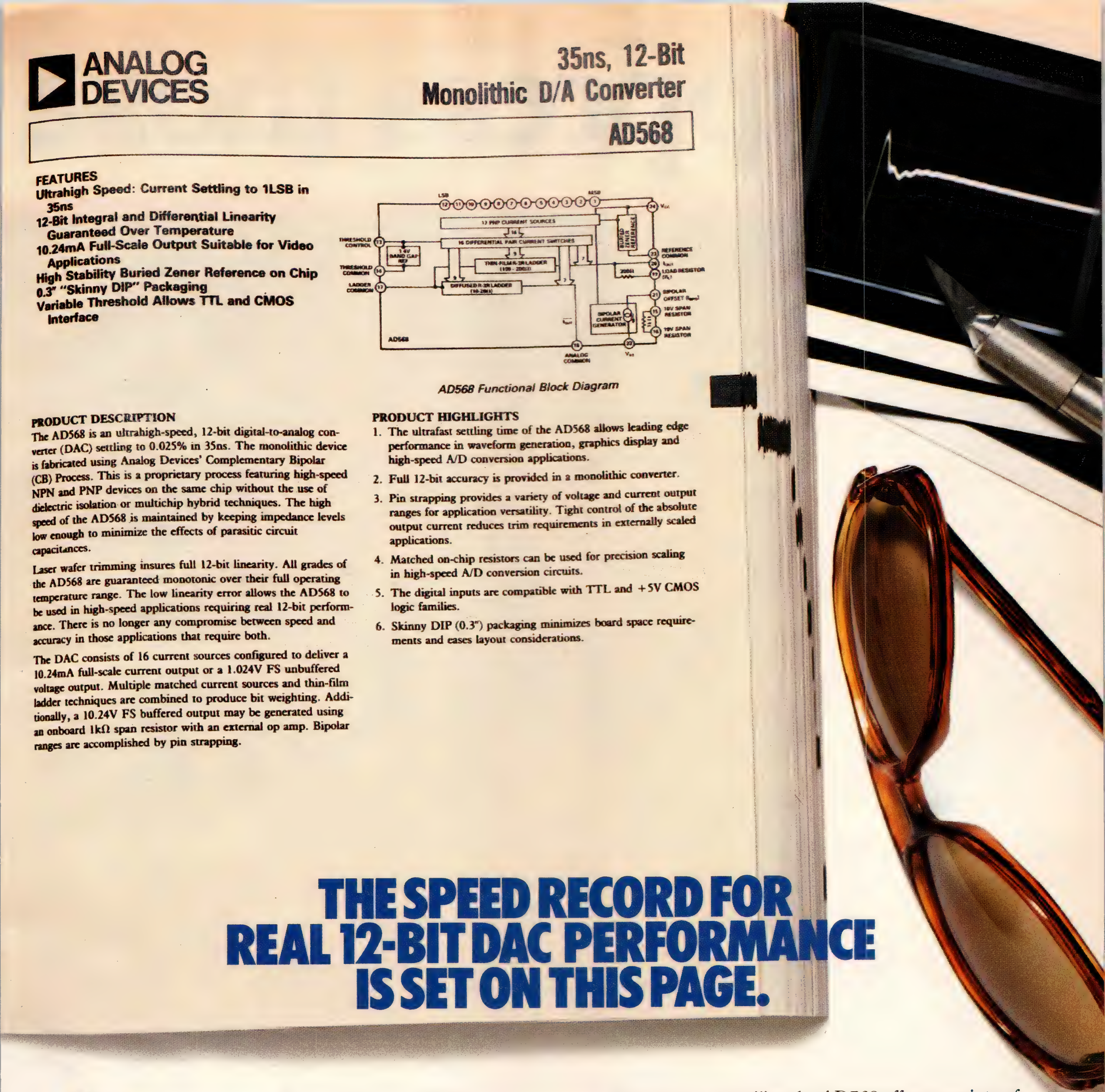
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AD568 Functional Block Diagram

PRODUCT DESCRIPTION

The AD568 is an ultrahigh-speed, 12-bit digital-to-analog converter (DAC) settling to 0.025% in 35ns. The monolithic device is fabricated using Analog Devices' Complementary Bipolar (CB) Process. This is a proprietary process featuring high-speed NPN and PNP devices on the same chip without the use of dielectric isolation or multichip hybrid techniques. The high speed of the AD568 is maintained by keeping impedance levels low enough to minimize the effects of parasitic circuit capacitances.

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PRODUCT HIGHLIGHTS

1. The ultrafast settling time of the AD568 allows leading edge performance in waveform generation, graphics display and high-speed A/D conversion applications.
2. Full 12-bit accuracy is provided in a monolithic converter.
3. Pin strapping provides a variety of voltage and current output ranges for application versatility. Tight control of the absolute output current reduces trim requirements in externally scaled applications.
4. Matched on-chip resistors can be used for precision scaling in high-speed A/D conversion circuits.
5. The digital inputs are compatible with TTL and +5V CMOS logic families.
6. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.

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CIRCLE NO 75

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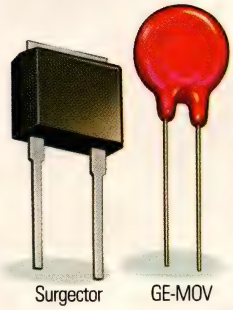

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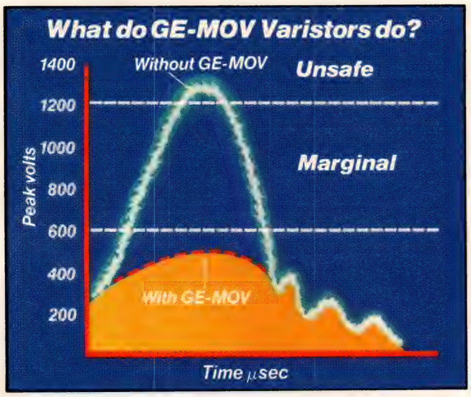

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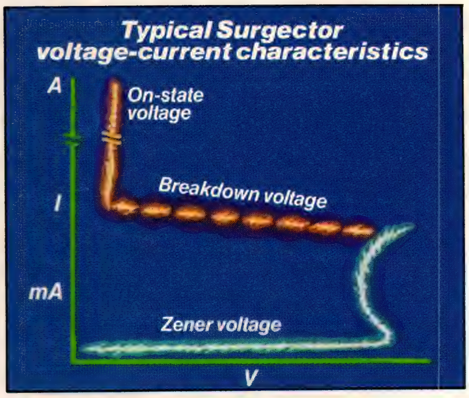

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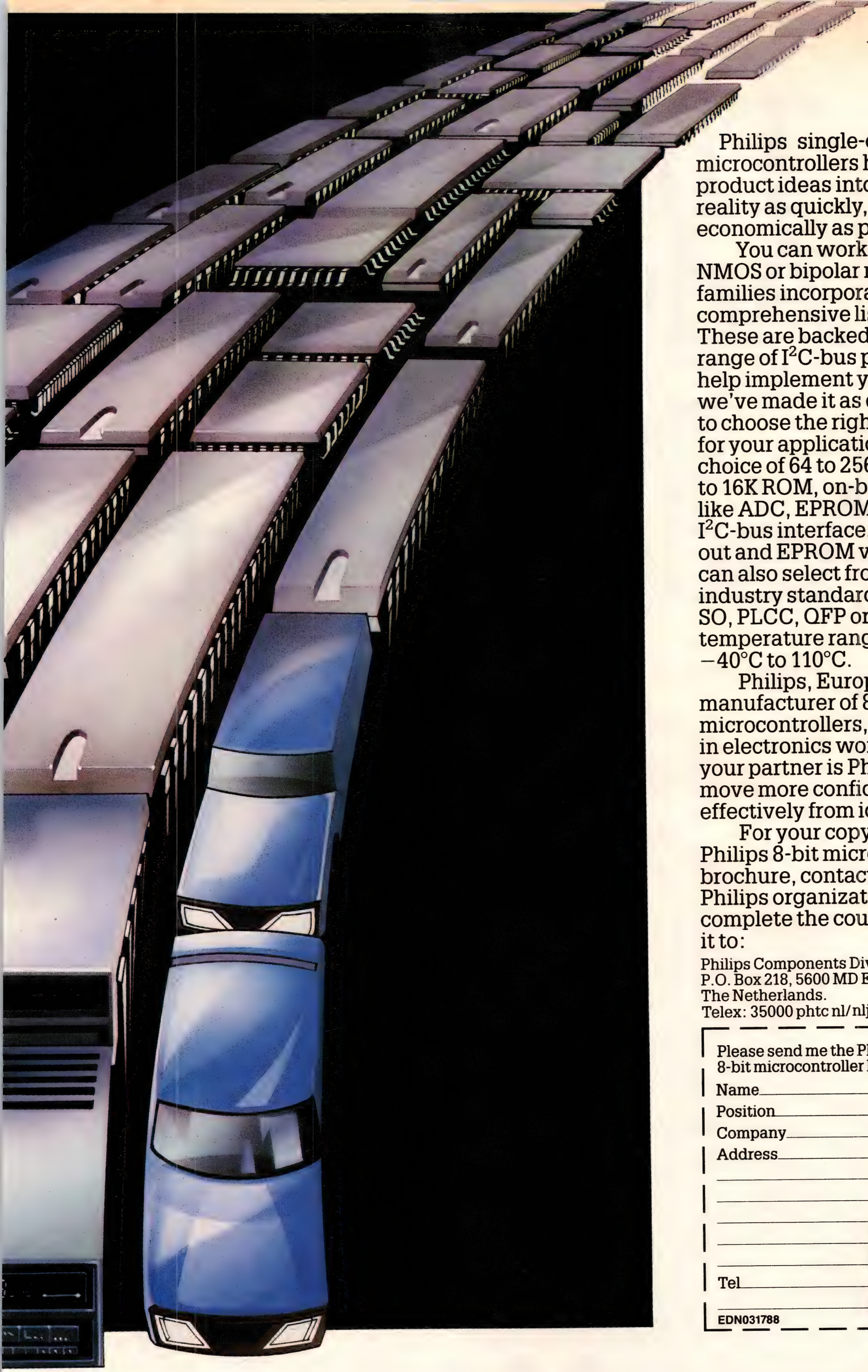

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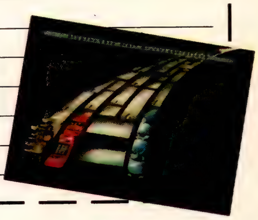

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CIRCLE NO 77

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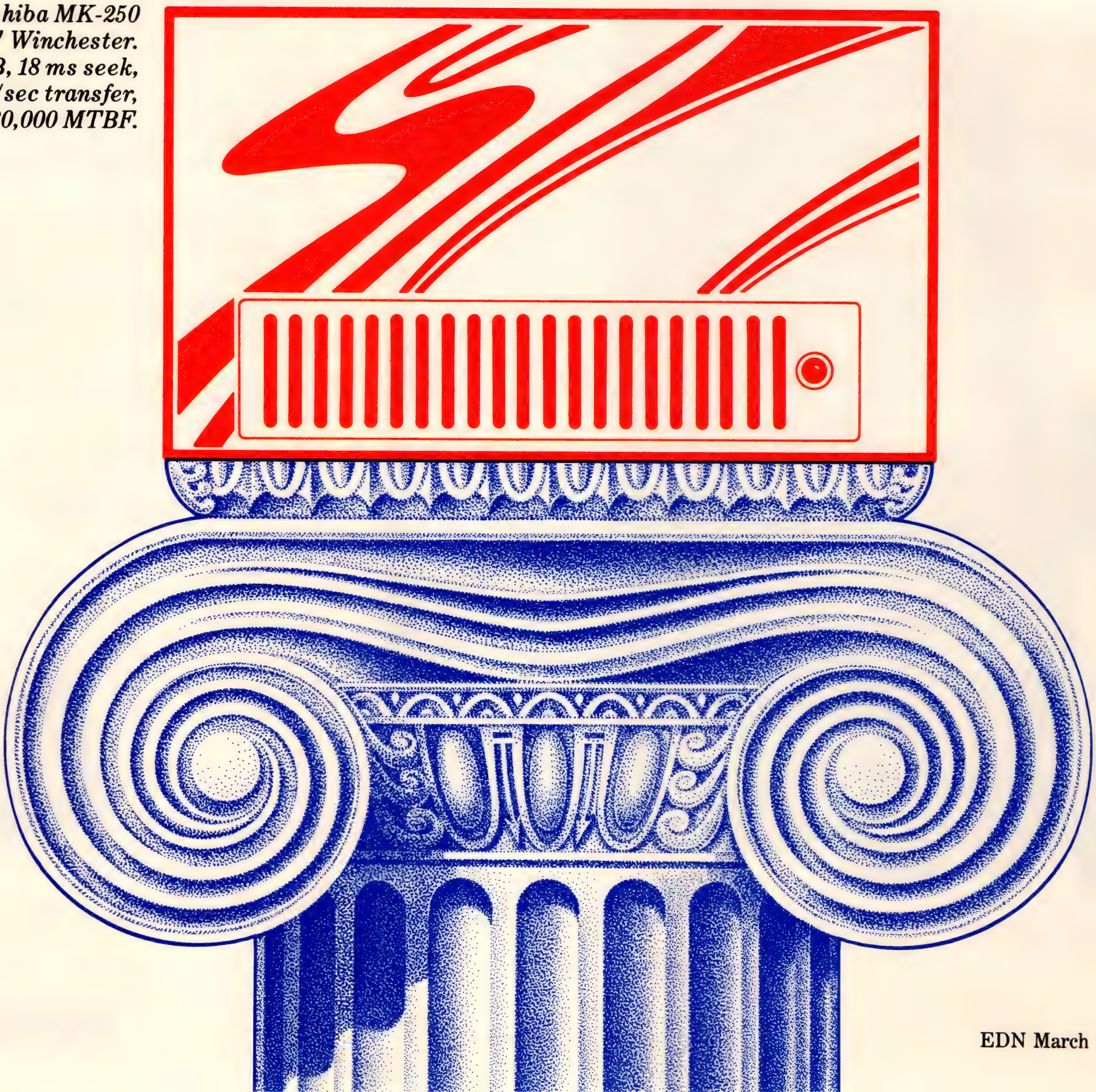

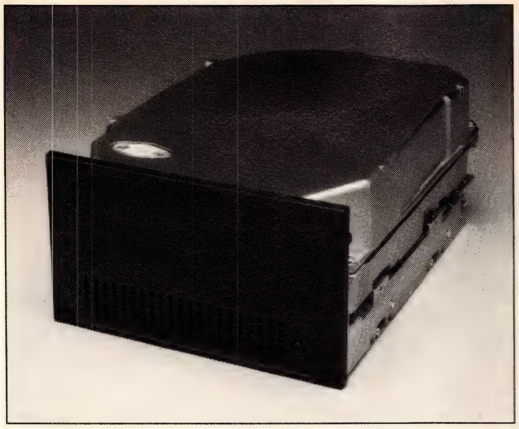

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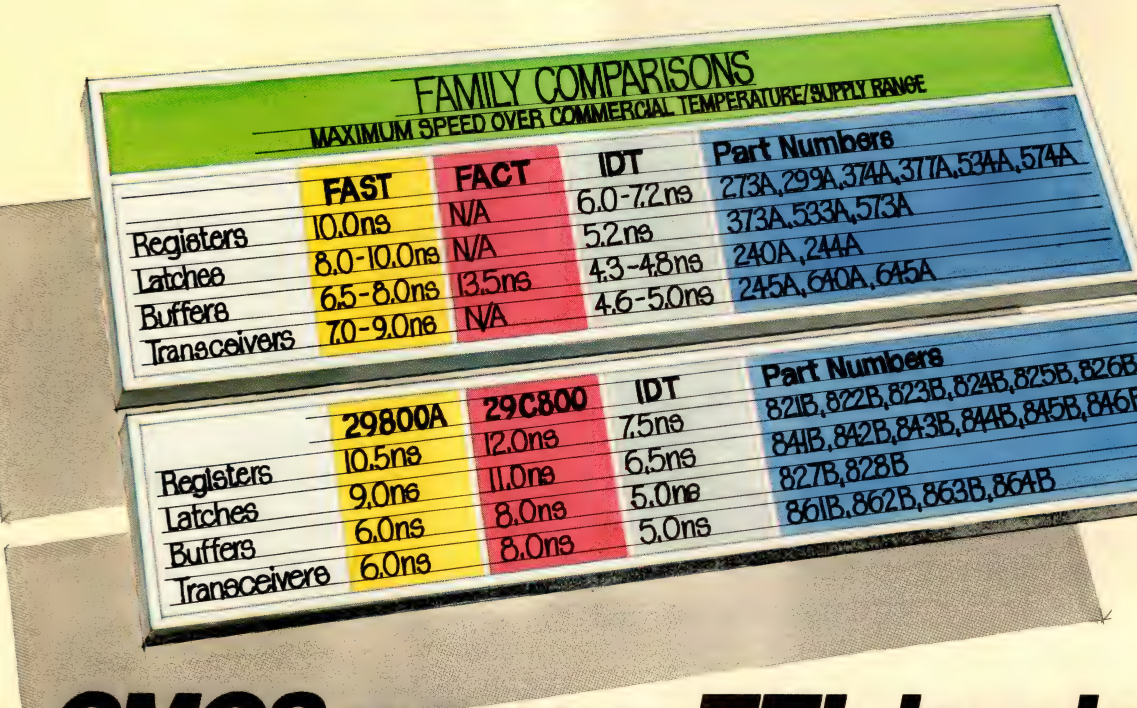

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Buffers	6.5-8.0ns	13.5ns	4.3-4.8ns	240A,244A
Transceivers	7.0-9.0ns	N/A	4.6-5.0ns	245A,640A,645A

	29800A	29C800	IDT	Part Numbers
Registers	10.5ns	12.0ns	7.5ns	821B,822B,823B,824B,825B,826B
Latches	9.0ns	11.0ns	6.5ns	841B,842B,843B,844B,845B,846B
Buffers	6.0ns	8.0ns	5.0ns	827B,828B
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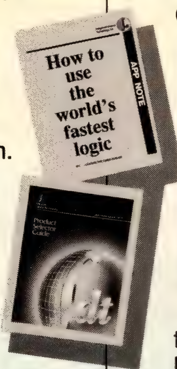

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CIRCLE NO 79

System architecture dominates design of no-wait-state cache

To extract maximum efficiency from today's 32-bit CPUs, you must provide them with zero-wait-state access to program and data memory. With μP clock speeds approaching 30 MHz, however, designing a cost-effective zero-wait-state memory is more difficult than ever.

James K Flynn and Narciso Mera,
AT&T Microelectronics

Dynamic RAMs can no longer support zero-wait-state accesses, and main memories built entirely from static RAMs are too expensive for today's low- to medium-performance computer systems. However, one way to achieve cost-effective, zero-wait-state performance is to combine a small, high-speed, static-RAM cache memory with a main memory based on a slower, less expensive dynamic RAM.

When considering such a memory architecture, however, you must evaluate several design options. In addition to choosing between a virtual and a physical cache, you must match your cache design to a CPU and memory-management unit (MMU). You must also consider the system-level impact of your operating system and application programs.

One of the first decisions you must make is between a combined MMU/CPU or separate unit approach. Your choice impacts not only your cache timing and expense, but your memory-management efficiency. In high-performance multiuser applications, designers generally opt for a separate CPU and MMU. That's because the separate MMU is able to store more virtual-address translation descriptors as well as support multiple users—both of which are essential for efficiently executing multiuser operating systems.

Having chosen a separate MMU and CPU, you must choose between a virtual and physical cache. A virtual cache stores virtual addresses and is located physically and logically between the μP and MMU. A physical cache stores the physical addresses it gets from the MMU's output.

To illustrate some of the tradeoffs, consider a virtual and physical cache implementation, both of which use Motorola's 68020 microprocessor and 68881 paged memory-management unit (PMMU).

Fig 1a shows a 68020 design with a virtual-address cache. The design assumes a 30-MHz clock frequency (approximately 30 nsec per clock cycle). Because the 68020 has a normal bus-read cycle of three clock periods, the memory system must supply valid data within 90 nsec for zero-wait-state read operations. **Fig 1b** shows the timing for a normal zero-wait-state bus cycle. The address is valid in the first clock period; the CPU reads data in the third period.

Because the virtual address from the CPU isn't valid until the end of the first clock cycle, to achieve a zero-wait-state access bus cycle, you must design the

You must match your cache design to a CPU and memory-management unit. Also consider the system-level impact of your operating system and application programs.

virtual cache so that it responds with valid data within 60 nsec (for cache hits). Assuming that the cache-control logic requires 30 nsec to make a hit/miss determination, the cache memory must have an access time of 30 nsec or less. You can design such a cache with fast CMOS static RAM at a cost of about $200 for a 64k-byte cache—roughly $150 for 30-nsec CMOS static RAM and $50 for the control logic.

Too slow for physical cache

Although it's feasible to implement a zero-wait-state *virtual* cache at 30 MHz using fast CMOS static RAM, such RAM is not fast enough for a *physical* cache using the same ICs (**Fig 2a**). The virtual-to-physical address-translation time, added by the MMU, delays the availability of a valid address until the end of the second clock period (**Fig 2b** shows the read-cycle timing for a physical cache). Consequently, to support a zero-wait-state access, the cache must respond in less than 30 nsec.

When you consider the delay that's inherent in the cache-control logic, only ECL static RAM can support zero-wait-state accesses at 30 MHz. A CMOS cache, in this application, sustains one or more wait states (inactive clock cycles) for each read operation.

Virtual vs physical cache

Although a virtual cache allows you to achieve zero-wait-state accesses with slower, less expensive memory, it also presents several design and performance obstacles—particularly in multiuser, multitasking, and multimaster applications. First, for some operating systems, you must design your system to handle cases where more than one virtual address maps into the same physical address (alias addressing). AT&T's Unix is one operating system that allows alias addressing; Berkley's System V Unix is one that does not.

Alias addressing is not a problem if the size of the virtual cache equals the page size used in the memory architecture. That's because only one cache entry can map to any given physical address. However, when the cache size exceeds the page size, two sections of code, or tasks, can access the same data using different

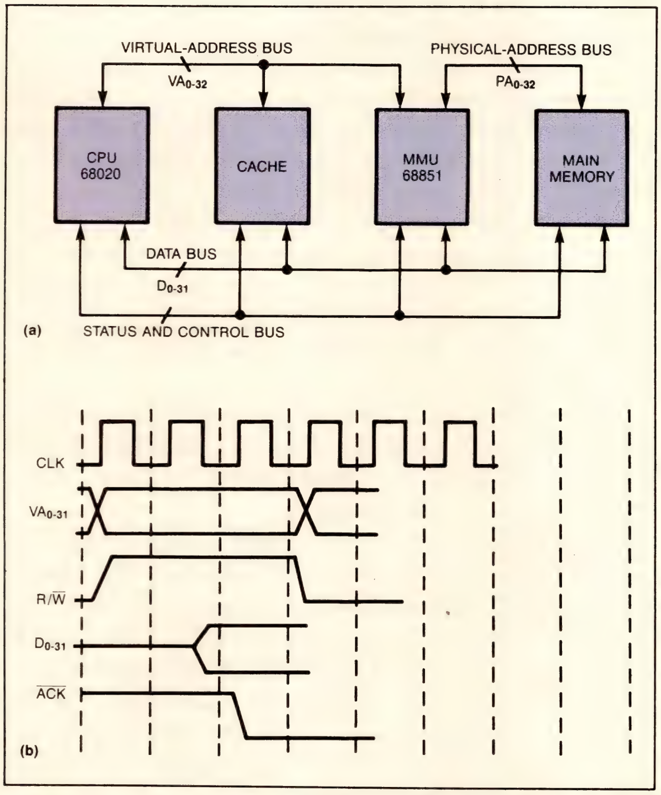


Fig 1—Because the 68020 has a normal bus-read cycle of three clock periods, *the memory system must supply valid data within 90 nsec for zero-wait-state read operations **(a)**; **(b)** shows the timing for a normal zero-wait-state bus cycle.*

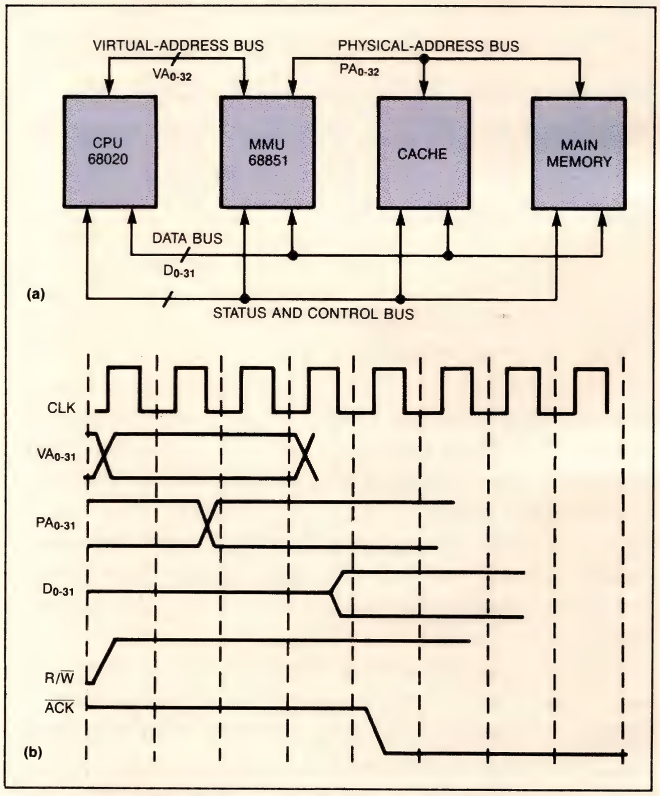


Fig 2—CMOS static RAM is not fast enough *for a physical cache using the same ICs as in **Fig 1a**. The virtual-to-physical address-translation time, added by the MMU, delays the availability of a valid address until the end of the second clock period **(b)**.*

Getting down to cache basics

A cache is a small array of high-speed semiconductor memory that designers typically use to economically reduce the effective time needed to access a larger, slower bank of memory (semiconductor or magnetic). The cache strategy relies on the locality of instructions and data. Operating systems and applications programs tend to spend large portions of time executing programs and accessing data in small sections of memory. As a result, a small cache can often sustain a high hit rate. As long as the hit rate is high, the effective memory access time for the entire memory mirrors that of the cache.

For a 16M-byte semiconductor address space, a 4k-byte cache is often sufficient to ensure a high hit rate. A 300M-byte disk, on the other hand, might merit a semiconductor cache of 1M byte or more.

A typical design

Fig A depicts a typical cache design. The cache consists of two sections of memory. The section on the right stores the cached data organized as eight entries of 8 bytes each. The section on the left contains a tag field for each 8-byte data entry. Address bits $A_{3\text{-}10}$ select the tag as well as the 8-byte data entry. Bits $A_{0\text{-}2}$ can select a byte within each entry, usually within a 32-bit word. The tag field stores the upper address bits for the 8-byte entry associated with each tag. This scheme allows any memory page or portion of a page to map into the cache.

In a system that uses a μP with 32 address bits, for example, the tag stores bits $A_{11\text{-}31}$ for each entry. The tag also includes other bit fields that signify status information, such as whether the entry is valid.

On a memory access, the cache-control logic compares the upper address bits presented on the μP address bus with the address stored in the cache tag. The tag entry corresponds to the entry selected by address bits $A_{3\text{-}10}$. A hit occurs when the μP address is the same as the tag address and the other tag fields indicate that the data are valid.

Other organizations possible

In this example, the cache is organized as 256 8-byte entries. However, you're free to use a variety of other configurations, as long as the cache is at least as large as the page size used in your memory system. If the higher-order address bit needed to distinguish between pages is of a higher order than the bit needed to distinguish between cache entries, then two addresses from the same page would map into the same cache address. Such a design limits cache effectiveness.

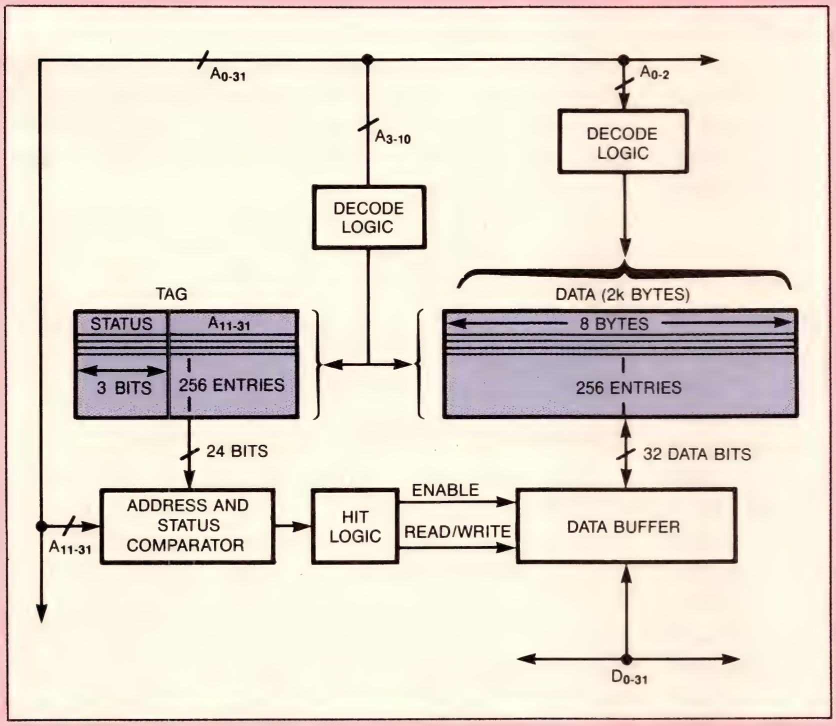


Fig A—This cache design *consists of two sections of memory: The section on the right stores the cached data organized as eight entries of 8 bytes each, and the section on the left contains a tag field for each 8-byte data entry.*

In high-performance multiuser applications, designers generally opt for a separate CPU and MMU.

virtual addresses mapped to the same physical location in the cache. One section can then read or write cache data without detecting changes made at the aliased address by the other section.

In a functionally similar case, a multiprocessor or multimaster design that uses a virtual cache must also be able to ensure data integrity when a second μP, or master, makes memory changes. For example, if your system uses a disk controller that performs DMA operations in physical memory, the system must be able to detect DMA transfers, because they may change the physical-memory contents that are also currently stored in the virtual cache. In such a situation, to ensure consistency between the cache and main memory, the system must invalidate cache entries that correspond to altered physical-address locations.

Maintaining data integrity

You can solve the integrity problem two ways. First, you can design the system so that the MMU handles all physical memory accesses. In this solution, even during a disk DMA operation, the μP's virtual-address bus carries virtual-address data automatically. The disadvantage is that it degrades performance. Each DMA operation incurs the additional delay of an MMU translation.

An alternative strategy is to add circuitry (a "bus watcher") to the cache to monitor the physical address bus for changes to data also contained in the cache. Upon detecting such a change, the bus watcher invalidates the appropriate cache entries.

Performance considerations in virtual caches

In addition to the problem of ensuring data consistency, using a virtual cache in a multiuser/multitasking system will present other design and performance challenges. First, you'll have to design the virtual cache to handle context switches. A context switch occurs in multiuser/multitasking systems when one task relinquishes control of the μP, and another task takes over.

Virtual caches may degrade system performance when accommodating context switches in a multiuser/multitasking system. In Unix applications, for example, though each task gets mapped to a different physical address space, several tasks may use the same virtual address space. Consequently, following a context switch, the cache may contain data that's not valid for the new tasks's virtual address space.

To prevent the new task from accessing invalid data, you must ensure that the task-specific portions of the cache are flushed when the operating system swaps that task out. You must also modify the operating system so that it issues a flush command after each context switch.

The problem with flushing and refilling the cache is degraded performance. The cache must be refilled one entry at a time, and main memory accesses typically require three to four wait states each. One way to reduce the overhead associated with flushing and refilling the cache is to design the system so that it leaves the operating-system kernel in the cache during context switches.

Naturally, the effect that context switches have on performance depends on your particular application. For example, consider a typical CAE-workstation application. Such a system may use Unix but primarily execute only one task at a time. Therefore, context switches don't occur often, and overhead associated with flushing and refilling the cache is negligible. In a business application, on the other hand, each user is given a small time slice and context switches occur more frequently. In this case, performance may suffer.

Physical cache eases context switches

Using a physical cache obviates flushing the cache after context switches. Because the cache stores physical addresses, it can't store aliased addresses, and each task maps into a different area of the physical address space. Consequently, no danger of a new task accessing invalid data exists.

The use of a physical cache also makes it easier to maintain data consistency between the cache and main memory. Because the physical cache resides on the address bus along with main memory, it is easier to design a circuit that monitors DMA transfers into main memory than a similar circuit for a virtual cache.

A combined CPU/MMU offers advantages

One way to obtain the data integrity and simplicity of a physical cache, without incurring the full penalty of address translation, is to use a combination MMU/CPU such as Motorola's 68030. By hiding address translation in its pipeline and eliminating the CPU-to-MMU interchip delay, the 68030 allows you to implement your zero-wait-state cache with slower, less expensive memory. With the 68030, virtual-to-physical address translation occurs within the μP, and a physical address appears on its external address bus.

While the CPU is executing one instruction, it fetches and loads the code required for the next one into its pipeline. Since the accesses required to fill the pipeline initially incur the full translation delay, one or more wait states result. However, once the pipeline is full, subsequent accesses can proceed with no wait states. The μP performs them concurrently with the execution of the current instruction, thereby hiding the translation delay.

The system experiences address-translation overhead only when the pipeline is empty, or following a branch—after which the μP must flush and refill its pipeline. The on-chip MMU also improves performance by eliminating the interchip delay between the MMU and CPU. This savings can eliminate a wait state for physical cache and main memory accesses, allowing you to use slower memory for a given performance level.

The penalty for using a combined MMU/CPU is reduced MMU capability. Because of IC-layout limitations, combined MMU/CPUs often compromise translation-buffer size. The translation buffer contains the descriptors that the MMU uses to translate virtual addresses to physical addresses. Where an external MMU can typically store descriptors for as many as 64 pages, combined CPU/MMUs such as the 68030 are typically limited to 22 descriptors.

Because the 68030 stores fewer descriptors, the probability of misses is higher. When the translation buffer does not contain the descriptor required for a given translation (a translation buffer miss), the MMU has to fetch the descriptor from main memory. A translation-buffer miss typically results in a system delay of 20 wait states.

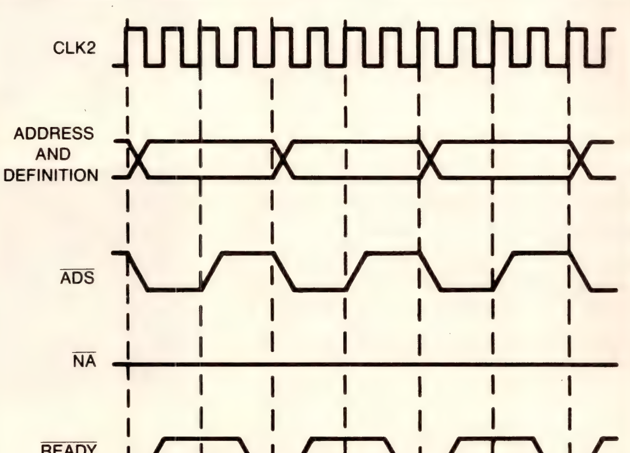


*Fig 3—**As long as the 80386's pipeline is full,** a valid physical address is available at the end of the clock period preceding the start of a bus cycle.*

Again, your application determines the importance of the translation buffer's size. Large multiuser applications, with several tasks executing simultaneously, require the translation buffer to map more pages of memory. In single-user PC applications, however, a small translation buffer probably won't have a significant impact on system performance.

Another popular CPU that includes a memory-management unit is Intel's 80386. Like the 68030, the 80386 hides address translation in its pipeline. The 80386's advantage is that, as long as the pipeline is full, a valid physical address is available at the end of the clock period preceeding the start of a bus cycle. Consequently, the memory system has two full clock periods to provide valid data (**Fig** 3 shows the read cycle timing). The 80386 allows you to use slower and less expensive cache memory than you can with the 68030.

Another way to eliminate the overhead of address translation without settling for a virtual cache is to employ the WE 32201 combination MMU/data cache. This IC eliminates the interchip delay between the MMU and the cache and also reduces address-translation overhead by performing translation in parallel with data-cache lookup.

In addition to providing high-speed, zero-wait-state accesses and data consistency, this combination MMU/data cache also offers smaller system size and lower cost. A cache implemented with discrete logic, programmable logic, and memory chips requires 3 in^2 of pc-board space for just its cache controller.

In addition to providing a 64-entry MMU, the WE 32201 has a 4k-byte, 2-way set-associative physical data cache that supports zero-wait-state accesses at speeds as high as 30 MHz. **Fig 4** shows a block diagram of the MMU/cache chip.

The WE 32201 uses two techniques to hide address translation and open the cache's access-time window. Rather than hiding address-translation time in the CPU, as combined CPU/MMUs do, the 32201 MMU/cache overlaps address translation with data-cache lookup. While the MMU portion of the chip translates address bits A_{11-31}, the cache controller uses address bits A_{0-10} to access one of two 2k-byte sets in the 4k-byte cache. The device can use the low-order bits for cache access while the upper bits are being translated, be-

While a virtual cache allows you to achieve zero-wait-state accesses with slower, less expensive memory, it also presents design and performance obstacles.

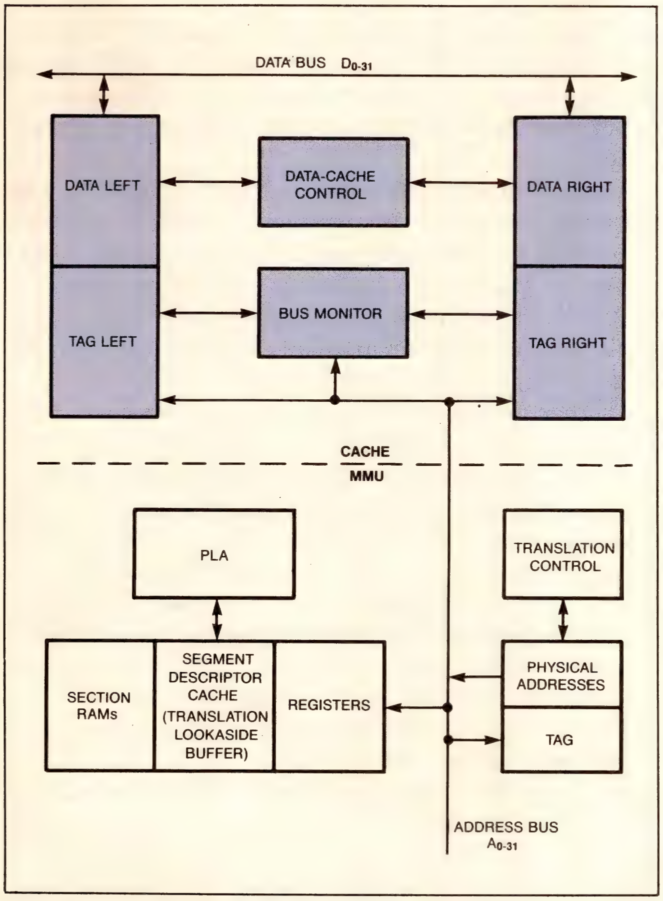


***Fig 4—In addition to providing a 64-entry MMU,** the WE 32201 provides a 4k-byte, 2-way set-associative physical data cache that supports zero-wait-state accesses at speeds up to 30 MHz.*

cause the lower address bits are simply an offset into the 2k-byte set and don't get modified during address translation.

Following address translation, the cache logic simply compares the physical address ($A_{11\text{-}31}$) with the address stored in the tag/data entry and selected by $A_{0\text{-}10}$. For hits, the cache presents valid data in the third clock period of the bus-read cycle (zero-wait-state access).

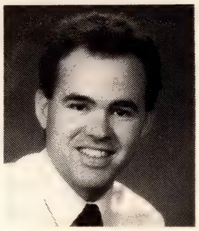
Built-in bus watcher

To ensure data consistency between the cache and main memory when the system has multiple processors and multiple masters, the WE 32201 combines a bus watcher to automatically monitor the physical address bus with a write-through feature. When a bus master, such as a DMA controller, accesses physical addresses in main memory, the cache automatically invalidates cache locations corresponding to them. For cache hits, the cache-control circuitry also updates the cache entry and sets its valid and most recently used flags.

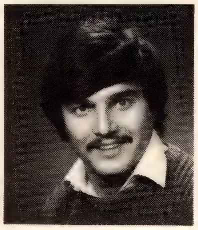
During CPU write operations, the system writes data through to main memory, whether a cache hit occurs or not. To maintain zero-wait-state 3-cycle operations in the event of a write-through, you must add buffer logic that completes the write to main memory. Your buffer logic latches the data, sends an acknowledge signal to the CPU, and continues the write operation to main memory. For write operations that do not generate a cache hit (misses), the CPU writes data only to main memory.

An alternative to write-through is the write-back design. In write-back schemes, the cache controller writes data only into the cache—and not main memory—on hits. This scheme simplifies normal write cycles for cache hits. However, following a context switch, or when a cache entry is replaced with data from a different address, the system must transfer the cache data to main memory before flushing the cache or replacing the entry. **EDN**

Authors' biographies



James K Flynn is a technical-product support engineer for microprocessors at AT&T Microelectronics (Holmdel, NJ). Jim has worked for AT&T since graduating from the Ohio Institute of Technology with a BSEE and the New Jersey Institute of Technology with an MCS. In his spare time, Jim enjoys skiing.



Narciso Mera is also a technical-product support engineer for AT&T Microelectronics. He obtained a BSEE from the Ohio Institute of Technology and an MCS from the New Jersey Institute of Technology. In his spare time, he enjoys skiing, fishing, and other outdoor activities.

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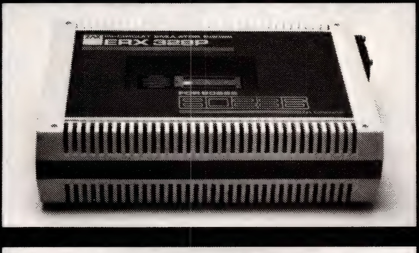

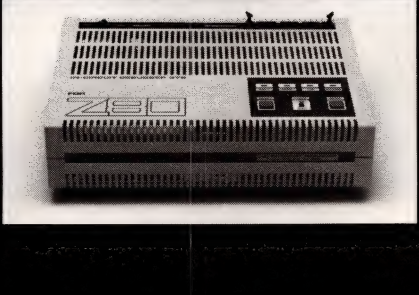

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Token-bus-controller interface must resolve family disparities

A system designed for a token bus network can benefit from a token bus controller such as the MC68824. The amount of glue logic required to interface the host to the controller will differ, however, depending on whether you're using an Intel or Motorola μP.

Paul Polansky, *Motorola Inc*

The MC68824 token bus controller (TBC) permits you to implement the media access-control sublayer of a token bus network based on IEEE Standard 802.4, which is part of a collection of standards for the Manufacturing Automation Protocol (MAP). The TBC uses an on-chip FIFO memory to queue data transmission on the network so it can share the local bus with a host μP (**Ref 1**). Because the TBC and the host mainly communicate through shared memory, the interface between the TBC and the CPU will vary, depending on your microprocessor—either an Intel 80186 or a Motorola MC68000, in this case. (For more information on the differences between the two types of μPs, see **box,** "Family differences can affect communications".)

The MC68824 basically adheres to Motorola's conventions, and thus designing an interface to an MC68000 μP is straightforward **(Fig 1)**. An address decoder creates a chip select ($\overline{\text{CS}}$) line by decoding the memory-mapped address lines for the TBC and conditioning them with the address-strobe ($\overline{\text{AS}}$) line. Most of the other signal lines connect directly to the TBC.

The data-transfer-acknowledge ($\overline{\text{DTACK}}$) line from the TBC ties directly to the system $\overline{\text{DTACK}}$ through a 3-state buffer that is in a high-impedance state when the TBC isn't selected. The bus-arbitration lines tie directly to the TBC. When the system has other bus masters, all of the $\overline{\text{BR}}$ lines are tied together and pulled up externally. Similarly, all of the $\overline{\text{BGACK}}$ lines are tied together. When other bus masters are present, the $\overline{\text{BG}}$ lines may be routed through a daisy-chained network or through a specific priority-encoded network. The address and data lines from the MC68000 also tie directly to their counterparts on the TBC. If the $\overline{\text{BGACK}}$ line is in an inactive high state, the peripheral drives it to an active low state to take control of the bus.

The TBC generates an interrupt to the CPU by routing its interrupt-request (IRQ) line to the appropriate input of a 74148 priority encoder. The encoded interrupt request appears on the interrupt control lines ($\overline{\text{IPL}}_{0\text{-}2}$). The interface circuitry then sends an interrupt-acknowledge ($\overline{\text{IACK}}$) signal back to the TBC by decoding the interrupt level being serviced on the address lines $A_{1\text{-}3}$ and gating this priority level with both the processor status lines ($FC_{0\text{-}2}$) and the $\overline{\text{AS}}$ line. An interrupt acknowledge occurs when the $FC_{0\text{-}2}$ lines are all at logical ones.

The TBC and the host communicate mainly through shared memory, so you must account for architectural differences.

Building an MC68824 interface for the 80186 µP requires more attention to the architectural differences between the two families. **Fig 2** depicts a block diagram of a relatively easy interface to construct. The design utilizes a CLK input to the TBC that is asynchronous with respect to the host processor clock. The TBC must have a clock rate equal to or greater than the 80186 to satisfy the bus-timing requirements. In this design, the

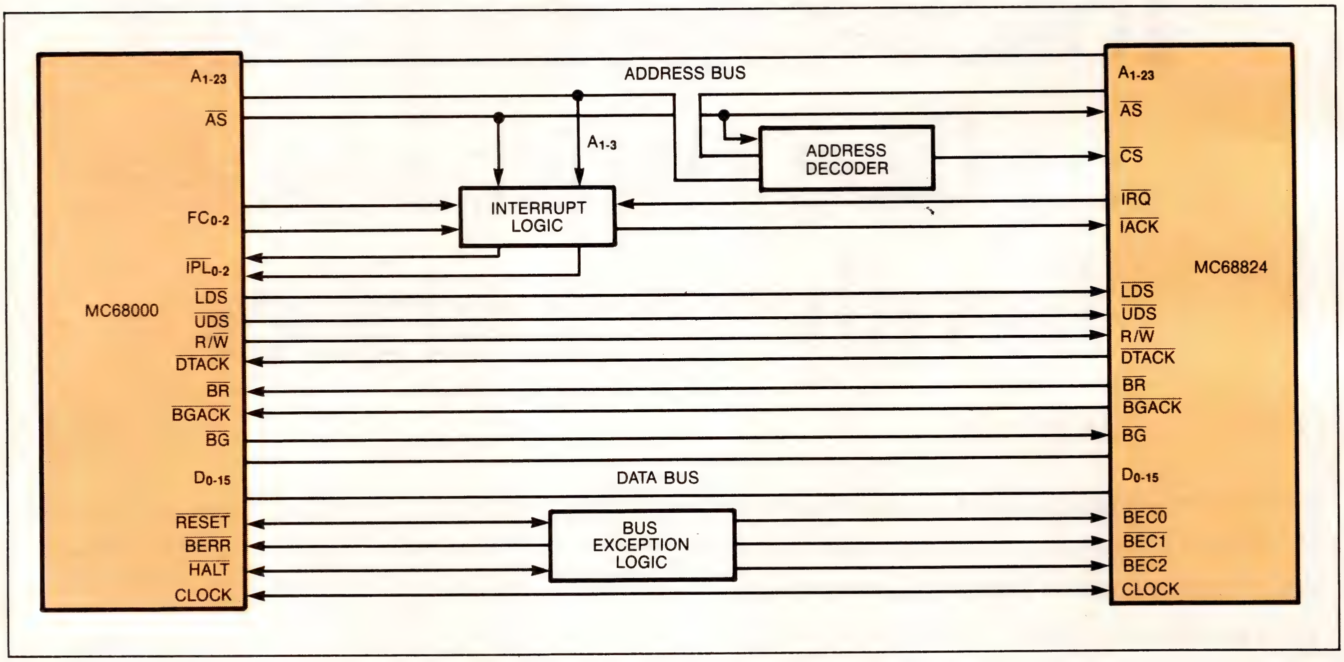

Fig 1—An interface for the MC68824 TBC to the MC68000 CPU requires minimal glue logic.

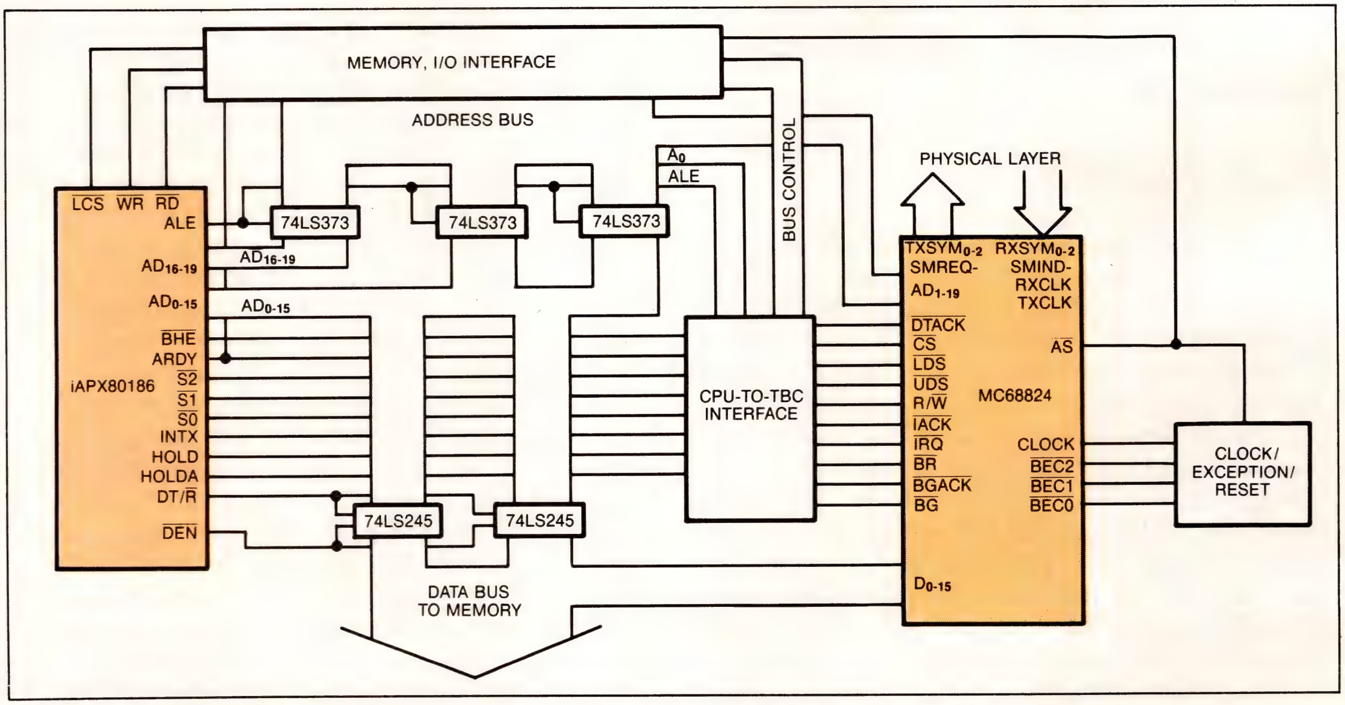

Fig 2—An interface for the MC68824 TBC to the 80186 CPU must demultiplex the addresses from the data.

clock rate is 12.5 MHz for the TBC and 10.0 MHz for the 80186. Incidentally, this interface is virtually the same for an 8086 CPU.

Because the 80186 multiplexes the address and data onto the same I/O lines, the interface requires 3-state latches to form the physical address bus, and isolation transceivers to form the physical data bus (**Fig 3**). The hold-acknowledge output command (HLDA) from the 80186 places the address latches (74LS373s) in a 3-state condition when the TBC has control. Similarly, the data-enable ($\overline{\text{DEN}}$) command from the CPU isolates the 74245 transceivers while the TBC has control.

Logic eases communications

Fig 4 shows the circuitry necessary for the 80186 to write to such registers in the TBC as the command register (CR), the interrupt-vector (IV) register, and two 16-bit sections of the 32-bit data register (DR). The circuitry also allows reading of the semaphore register (SR), execution of bus arbitration, and servicing of an interrupt.

A 1-of-8 decoder (74138) decodes the three status lines ($\overline{\text{S}}_{0\text{-}2}$) to generate the R/$\overline{\text{W}}$ signal to the TBC. The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals from the CPU are not used to develop R/$\overline{\text{W}}$, because the R/$\overline{\text{W}}$ signal must be valid before the upper and lower data strobes ($\overline{\text{UDS}}$ and $\overline{\text{LDS}}$) are asserted in the Motorola architecture. Using the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals would require delaying the $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ commands an extra clock period to meet the 20-nsec setup-time requirement of the TBC. The Intel μP's architecture provides the information early enough on the status lines to avoid this problem. The design is suitable for either memory or I/O mapping; however, memory mapping allows software to be written in a machine-independent language, such as C.

This design also supports autovectored interrupts in the fully nested mode of the 80186. When acknowledging an interrupt, the 80186 executes two consecutive $\overline{\text{INTA}}$ cycles; the CPU reads the interrupt vector on the second cycle. During this time, the TBC can provide one of two possible interrupt vectors to the host. The TBC reserves one vector for a severe bus error or address error interrupt. A severe interrupt indicates that a bus or address error has occurred twice consecutively without the host taking appropriate action. All of the other interrupts use the second reserved vector. In

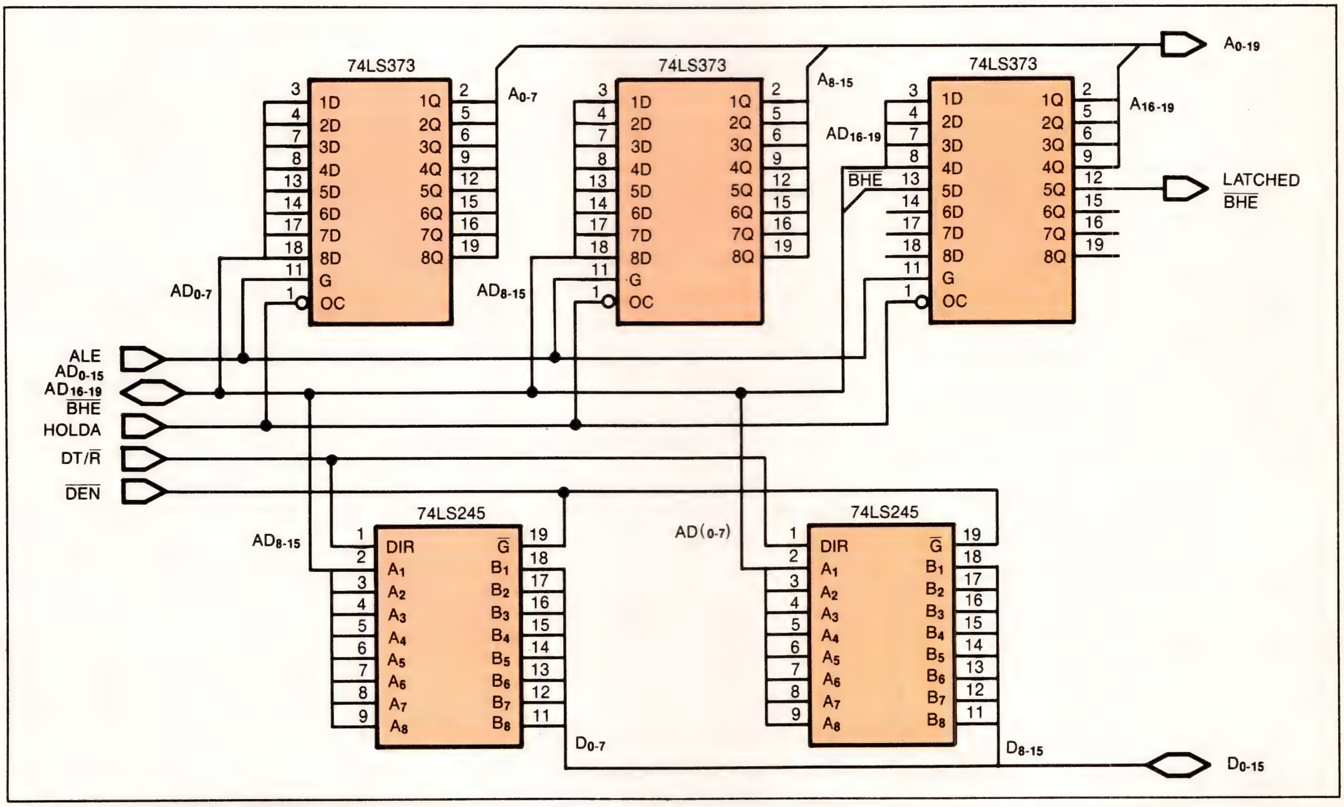

Fig 3—Three-state latches and 3-state transceivers create the physical address and data buses.

The interface requires 3-state latches to form the physical address bus, and isolation transceivers to form the physical data bus.

addition, a bus or address error can be detected by examining the BAERR bit in the TBC's interrupt status word 0.

The TBC interface develops Motorola's $\overline{\text{UDS}}$ command from Intel's $\overline{\text{BHE}}$ command, and it develops Motorola's $\overline{\text{LDS}}$ command from Intel's A_0 command. The $\overline{\text{UDS}}$ and the $\overline{\text{LDS}}$ signals represent transfers on the upper and lower eight bits of the data bus, respectively. The 74374, labeled Latch$_1$ in **Fig 4,** latches the $R/\overline{W}$, $\overline{\text{UDS}}$, $\overline{\text{LDS}}$, A_1, and A_2 signals on the falling edge of the address latch enable (ALE) command. The latched outputs of the $R/\overline{W}$, A_1, and A_2 lines connect directly to the TBC to meet the setup-time requirements. Then, the falling edge of the clock line from the CPU gates the remainder of the signals to the TBC.

When the ALE line is high, the outputs of Latch$_1$ are in a 3-state condition, permitting the $\overline{\text{UDS}}$ and the $\overline{\text{LDS}}$ lines to be inactive for at least one clock period before enabling Latch$_1$'s outputs, which satisfies a timing requirement of the TBC. The other latch, labeled Latch$_2$ in **Fig 4,** latches the inactive state of the $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ lines until the next clock edge makes these lines active. It is this timing restraint that forces the clock rate of the TBC to be equal to or greater than the CPU's clock rate.

Don't forget bus arbitration

The bus-arbitration scheme roughly corresponds to the one used in the MC68000 design, but it is not a perfect analogy. The HOLD command, which is analogous to the $\overline{\text{BR}}$ command, must remain active the entire time that an alternate bus master controls the bus. The

Family differences can affect communications

Two popular 16-bit μP families are Motorola's MC68000 and Intel's 8086/80186. The processors' architectures differ in certain key aspects, however, which demand attention when you're designing a communication interface for an MC68824 TBC. Intel, for example, multiplexes its address and data buses; Motorola uses separate address and data buses. The byte-ordering convention is also different. In the Motorola convention, the high-order byte occupies the lower memory address, whereas in the Intel architecture, the high-order byte appears in the higher memory address **(Fig A).** The communication interface must account for these and other anomalies.

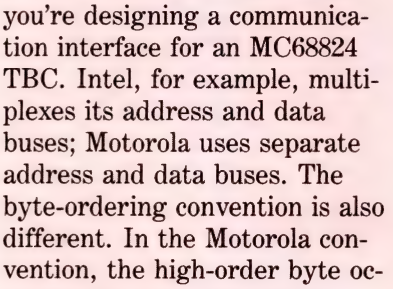
D_{15} • • • D_8 D_7 • • • D_0
MOTOROLA CONVENTION
BYTE 0
BYTE 1
D_{15} • • • D_8 D_7 • • • D_0
INTEL CONVENTION
BYTE 1
BYTE 0

Fig A—Motorola and Intel have different *conventions for placing bytes in memory locations.*

When an MC68000 or an 80186 performs a 16-bit-word memory access, the disparate ordering conventions aren't a problem because both even- and odd-byte memory locations are selected, and it doesn't matter which section of memory is called even or odd. However, byte accesses and accesses to serial data do require attention.

The ordering convention also affects long-word (32-bit) memory accesses, such as a pointer stored in the TBC's initialization table. The Motorola convention expects the high order word in the higher memory address (that is, the lowest order byte in address 0, the next in address 1, the third in address 2, and the highest order byte in address 3). The order for the bytes of a long word is reversed for the Intel convention. Your interface design must account for these differences.

The 16-bit organization and segmented addressing of the 80186 vs the 32-bit organization and linear addressing of the MC68000 also affects the design of an interface for the TBC. The 80186 provides a 20-bit address space by adding a 16-bit segment register shifted left by four bits to the 16-bit logical address register. This address space subdivides into memory and I/O space. The MC68000 has 32-bit registers and supports 24 lines of linear addressing. The MC68824 contains 32-bit internal pointer registers designed to handle a 32-bit address bus for linear, nonsegmented addressing.

Diplomatic interruptions

The μP families also differ in their methods of handling interrupts. The Motorola family has two options for interrupts: regu-

$\overline{\text{BR}}$ line from the TBC becomes inactive shortly after the TBC takes control of the bus. Therefore, the $\overline{\text{BR}}$ line and the $\overline{\text{BGACK}}$ line from the TBC connect to a NAND gate with an output latch to form the HOLD command. Also the 80186 requires the HOLD command to be inactive for at least one clock period plus 25 nsec before the next falling clock edge occurs for internal synchronization. This requirement corresponds to an inactive HOLD time between 125 and 225 nsec when the 80186 runs at 10 MHz.

The halt-generator enable mode of the TBC places another constraint on the interface design for the HOLD command. This mode limits a DMA burst to eight consecutive cycles when the SET MODE 3 command enables the HLEN bit in the command register. At the end of the burst, the TBC relinquishes the bus. If more cycles are needed, the TBC reasserts the $\overline{\text{BR}}$ line in at least one and one-half clock periods plus 20 nsec. Therefore, the HOLD command to the CPU must remain active until the HOLDA line becomes inactive.

The generation of the $\overline{\text{BG}}$ signal to the TBC also requires some attention. While the TBC is in the halt-generator mode, it must relinquish the bus after eight consecutive DMA cycles, and therefore one DMA burst may not fill up or empty the TBC's FIFO buffer. Under these circumstances, if the CPU gives it permission, the TBC will want to re-establish control of the bus.

The TBC timing requires that the $\overline{\text{BG}}$ line is valid only until the $\overline{\text{BR}}$ line becomes inactive. However, if the TBC reasserts the $\overline{\text{BR}}$ line before the CPU invalidates the $\overline{\text{BG}}$ line, the TBC will recognize that $\overline{\text{BG}}$ is valid and

lar (vectored) and autovectored. The regular interrupts are encoded as priority levels on lines $\text{IPL}_{0\text{-}2}$; level 7 ($\text{IPL}_{0\text{-}2}$=000) is nonmaskable. The MC68000 enters an interrupt acknowledge cycle by setting the $\text{FC}_{0\text{-}2}$ lines to 111. The interrupting source places its vector on data lines D_0 through D_7 and terminates the cycle with $\overline{\text{DTACK}}$. In the autovectored mode, the interrupting source asserts $\overline{\text{VPA}}$ during an interrupt cycle instead of $\overline{\text{DTACK}}$. This assertion causes the CPU to fetch a priority-based vector.

The Intel family handles vectored and autovectored interrupts in one of several modes. The 80186 offers a mode compatible with the iRMX86 operating system as well as a master mode. In the master mode, different configurations of the interrupt lines permit the use of either four request lines or two request and two acknowledge lines.

In the vectored mode, the CPU runs two consecutive interrupt acknowledge cycles. During the first cycle, the μP informs the system that it is acknowledging an interrupt. During the second cycle, the interrupting source places its vector type on the lower half of the data bus. The CPU uses the vector type to access a vector table. When the 80186 is in a fully nested mode, the CPU responds to autovectored interrupts.

Impartial arbitration is best

Both families have bus-arbitration schemes that allow an alternate source to request control of the bus. In the Intel scheme, the requesting device asserts a HOLD signal and then waits for the host to assert a HOLDA signal before taking control of the bus. The alternate bus master must assert the HOLD command for the entire time it owns the bus. When there are multiple bus masters, the scheme requires an external arbiter.

In the Motorola scheme, the requesting device asserts the $\overline{\text{BR}}$ line and waits for the host to assert the $\overline{\text{BG}}$ command. The requesting agent then samples the state of the $\overline{\text{BGACK}}$ and $\overline{\text{AS}}$ signals to ensure that no other device is using the bus. When both lines are inactive, the agent asserts $\overline{\text{BGACK}}$, deactivates $\overline{\text{BR}}$, and starts running its own bus cycles. The bus master asserts $\overline{\text{BGACK}}$ for the entire time that it controls the bus.

The highest level of exception handling in the Intel architecture is the nonmaskable interrupt. The hardware uses this interrupt to initiate processing of an exceptional condition on a high-priority basis at the end of the current bus cycle. In the Motorola architecture, a bus exception terminates the current bus cycle with or without the $\overline{\text{DTACK}}$ signal.

A severe interrupt indicates that a bus or address error has occurred twice consecutively without the host taking appropriate action.

will assume control of the bus without permission. Therefore, the $\overline{BR}$ line from the TBC clears the $\overline{BG}$ command to the TBC when the $\overline{BR}$ line becomes inactive. In addition, the TBC monitors the $\overline{BGACK}$ and the $\overline{AS}$ lines before asserting $\overline{BGACK}$ to take control of the bus.

The memory map and the memory controller and chip-select logic are shown in **Figs 5** and **6,** respectively. Memory location $FFFF0 contains the initial instruction for the 80186 µP, with room in the higher memory space for the system software. The low-RAM space contains the stack and the interrupt vector table for internally generated vectors. You can add additional RAM in the gap of the address map for more shared memory space. A0000 is the offset base address for the TBC in the memory map. In this example, the TBC occupies 64k bytes in the memory space; its internal registers are mapped from A0000 to A0006. An access to any address in the TBC's memory space enables the $\overline{CS}$ line to the TBC.

The memory-access circuitry of **Fig 7** illustrates another architectural difference between the Intel and Motorola µP families that affects the design of a TBC. The Motorola convention accesses memory by asserting the $R/\overline{W}$ signal to initiate the sequence. The $R/\overline{W}$ line ties directly to the $\overline{WE}$ line on the memory chips and to an inverter whose output ties directly to the $\overline{OE}$ line on the memory chips. Subsequently, data strobes and memory chip-select decoders generate a $\overline{CE}$ signal to access the data.

Memory accesses are different

In contrast, the Intel convention first decodes the memory-select lines to assert the $\overline{CE}$ command. Subsequently, the $\overline{RD}$ line (which connects to the $\overline{OE}$ line on the memory chips) or the $\overline{WR}$ line (which connects to the $\overline{WE}$ line on the memory chips) accesses the data. The logic circuitry shown in **Fig 6** drives the memory-interface circuitry in **Fig 7** to accommodate both conventions.

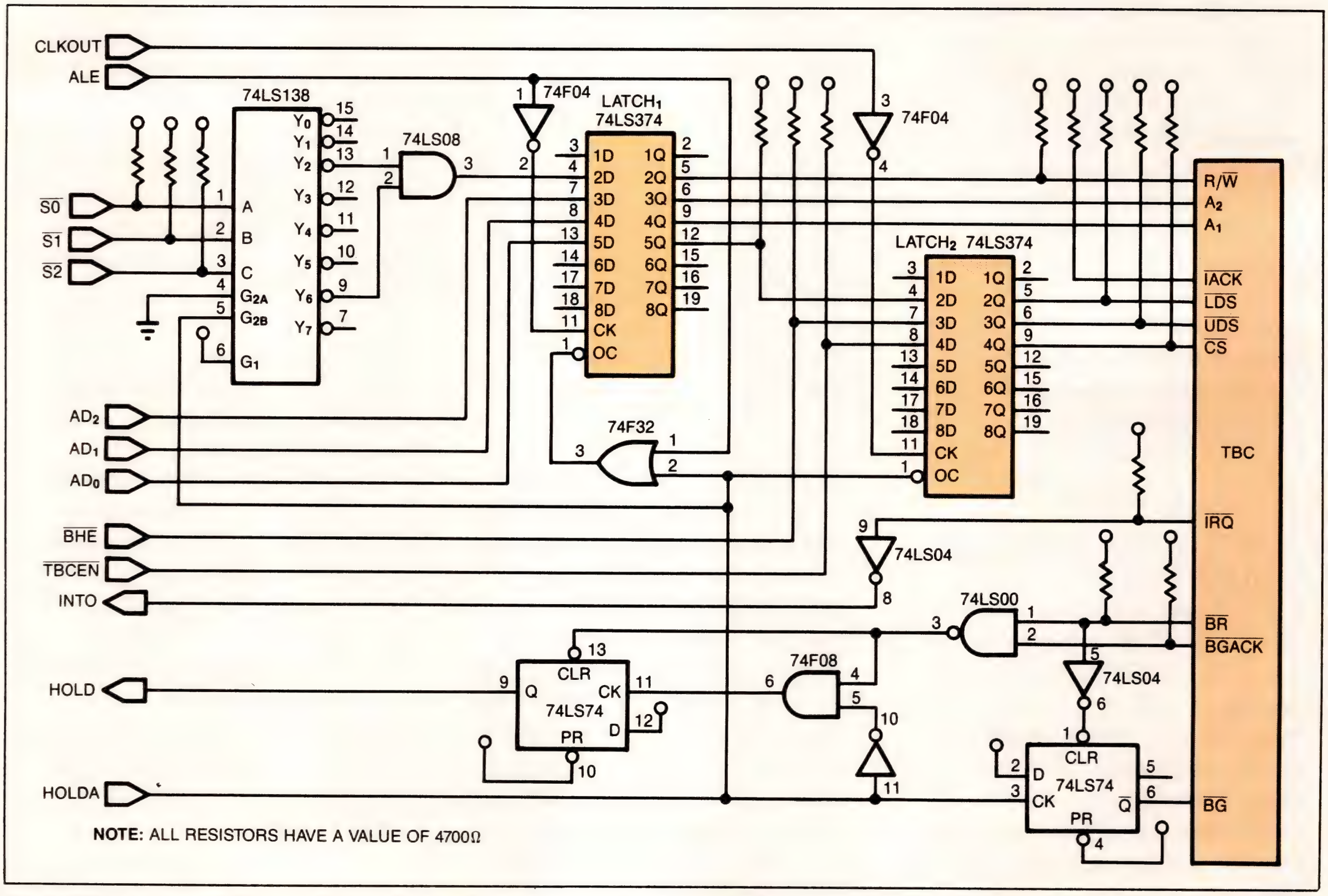

***Fig 4—This schematic diagram depicts the glue logic** necessary for 80186 and MC68824 communications.*

The design must also account for differences in the byte-ordering conventions of the two families. Byte ordering is critical in a serial system where you must maintain the sequence of successive bytes. The host μP can run a byte-swapping routine in software, but this routine requires valuable CPU time. The MC68824 has an optional feature, however, whereby this task is performed automatically. The user accesses this feature in software by setting the SWAP bit in the SET MODE 3 command to the TBC. This capability only applies to data buffers, though, because the byte order isn't important for other shared memory locations for the TBC.

You must partition the shared memory space of the TBC interface to accommodate each peripheral. The upper address bits (A_{17}, A_{18}, A_{19}) select the boundaries in the memory space for the DUART, TBC, ROM, and RAM. A 1-of-8 decoder (74LS138) develops the respective enable commands, which are labeled $\overline{\text{DUARTEN}}$, $\overline{\text{TBCEN}}$, $\overline{\text{ROMEN}}$, and $\overline{\text{RAMEN}}$ **(Fig 6).**

Except for $\overline{\text{TBCEN}}$, the design also uses these commands to create an active high asynchronous ready (ARDY) signal with no wait states for the RAM and with one wait state for the EPROM in order to terminate bus cycles. **Fig 8** shows the sequential circuitry necessary to perform a logical NAND operation on the $\overline{\text{RAMEN}}$, $\overline{\text{ROMEN}}$, DUARTEN, and $\overline{\text{DTACK}}$ line to develop the ARDY signal. The $\overline{\text{DTACK}}$ line is an input line to the CPU when the TBC is the bus master, and it is an output line to the TBC when the host is the master. The 74365 3-state latch avoids any contention for the $\overline{\text{DTACK}}$ signal.

Fig 9 depicts the bus exception and reset circuitry for the TBC. The $\overline{\text{RESET}}$ line drives a 74LS148 priority encoder to command a reset condition on the $\overline{\text{BEC}}$ line to the TBC (all zeros). The $\overline{\text{BERR}}$ line drives the same priority encoder to signal the TBC on the $\overline{\text{BEC}}$ lines that a bus error has occurred. The $\overline{\text{BERR}}$ line acts as a

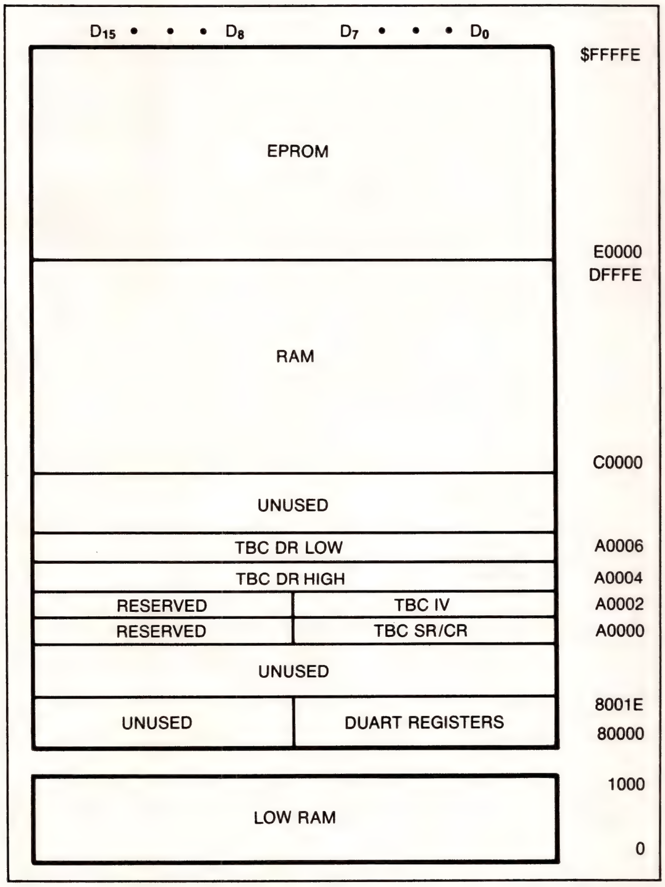

__Fig 5—The memory map places the interrupt vector table and stack in low RAM.__ The map places the DUART registers after the gap followed by the TBC, RAM, and EPROM.

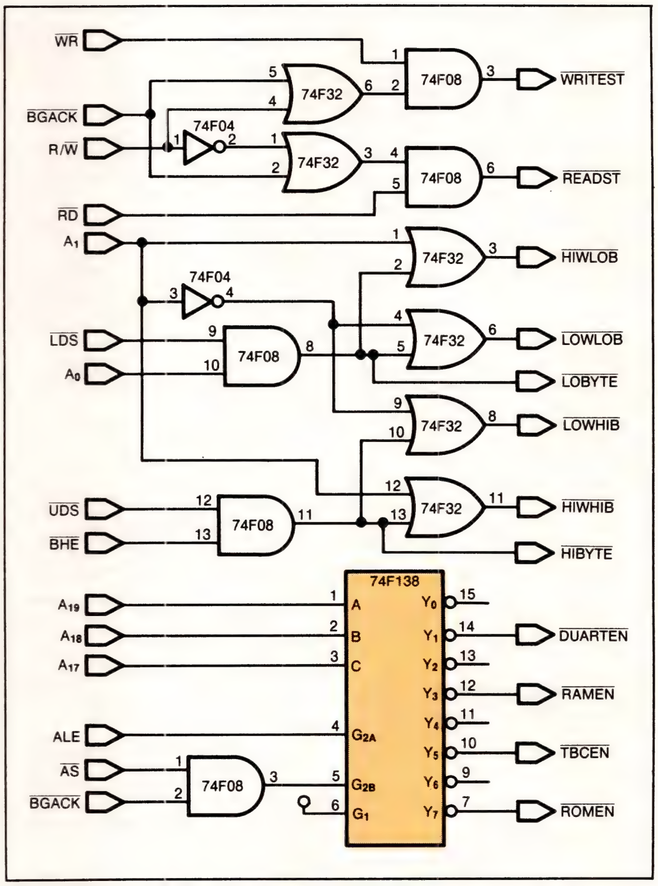

__Fig 6—The memory controller for developing the signals necessary__ to access memory uses simple logic gates and a 74F138 1-of-8 decoder.

If you write the application software in C, you must pay attention to pointers stored in memory.

timeout signal when the TBC tries to access a device other than the static RAM.

If you write the application software in C, you must pay attention to pointers stored in memory because the 80186 has a segmented architecture and a 16-bit internal organization, whereas the MC68000 has a linear,

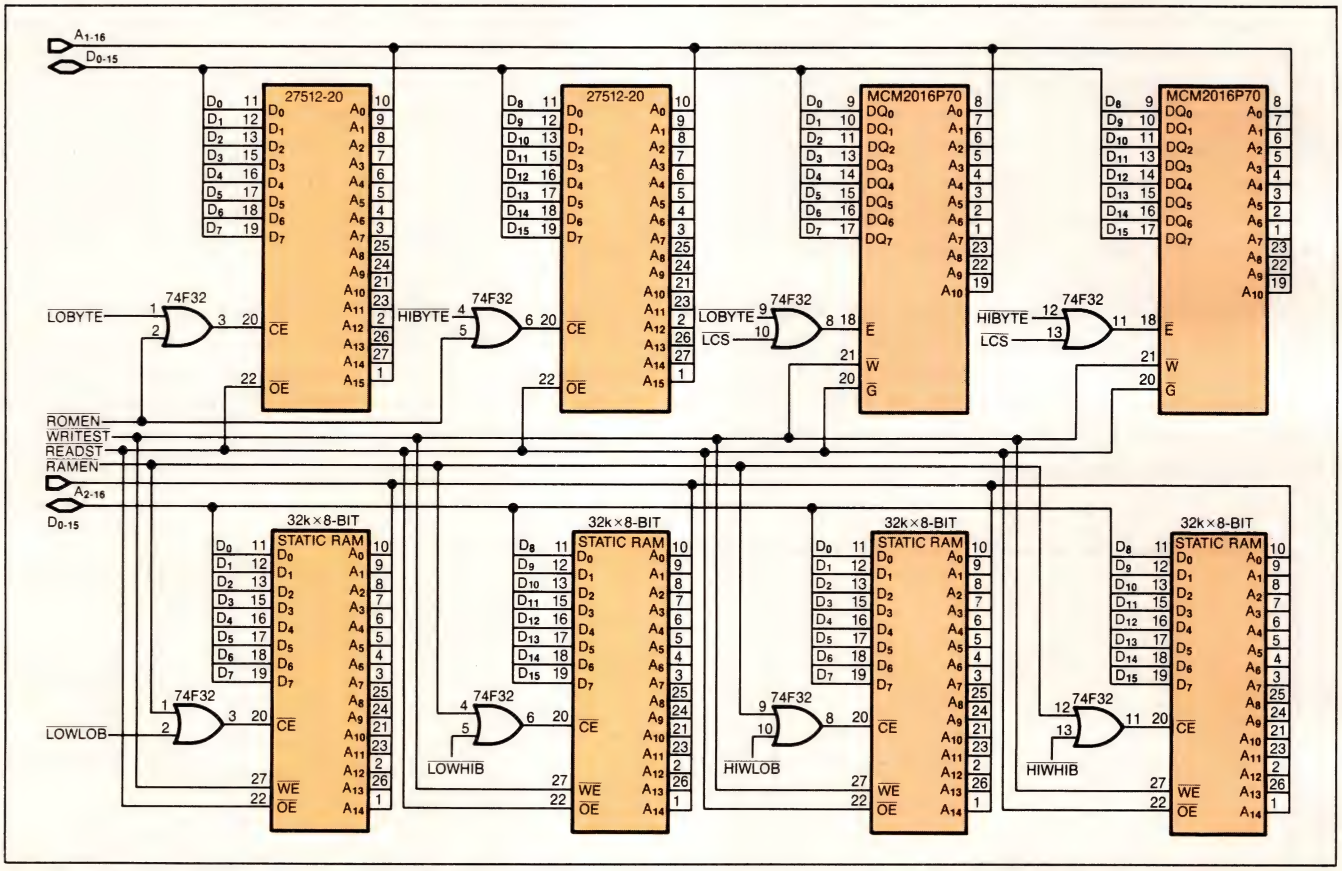

Fig 7—This memory interface is compatible *with the TBC-interface design for both the MC68000 and the 80186 μPs.*

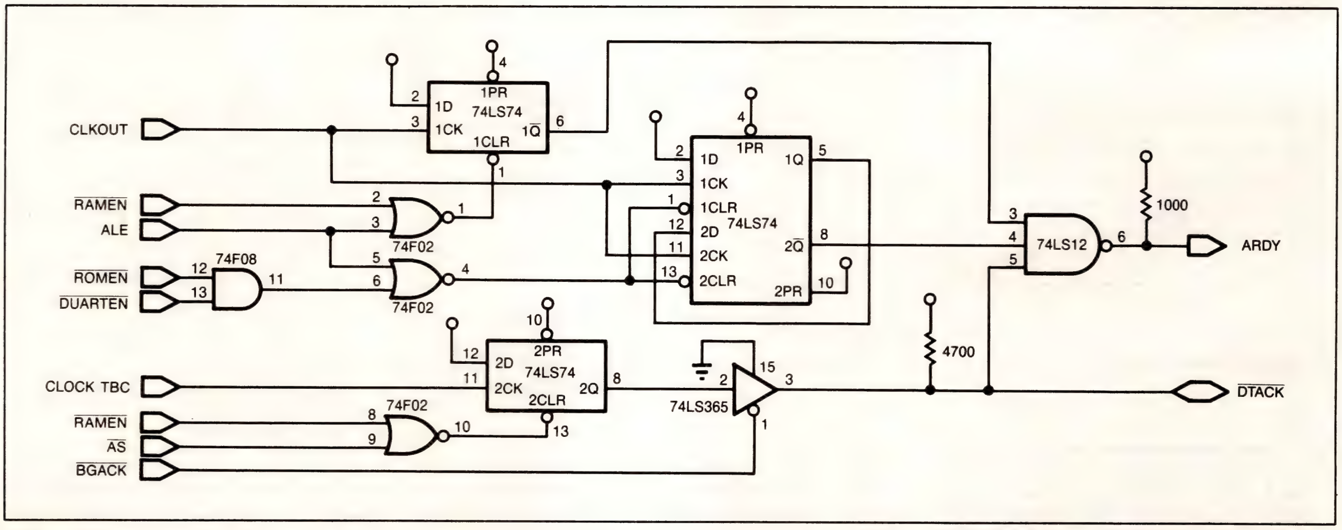

Fig 8—This schematic illustrates the sequential *and level logic required to create the ARDY and $\overline{DTACK}$ lines.*

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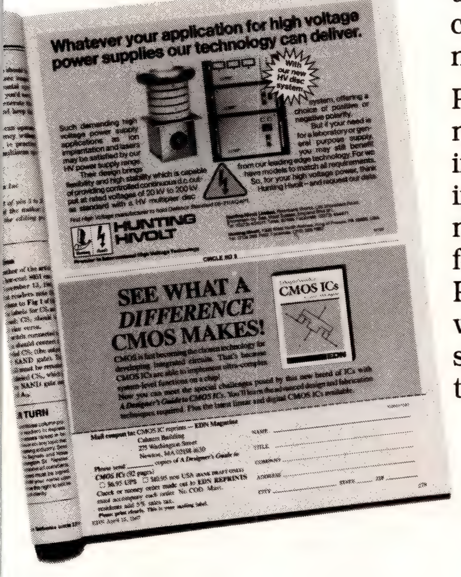

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The TBC should be given a high priority on the local bus because of the real-time nature of the token bus medium.

32-bit internal organization. A pointer for the 80186 is stored in memory as an offset in the first word, followed by a segment in the second word. In the MC68000 and TBC structure, a pointer is stored as a 32-bit linear address with the high address word stored in the first memory location, and the low address word stored in the second memory location.

The application software must reconcile these differences. Software written for the 80186 must initialize a TBC pointer by converting the segmented address to a linear 32-bit address. This requires a routine—call it int_to_mot()—which takes a 2-word pointer in Intel format and converts it to Motorola format. Similarly, a routine called mot_to_int(), converts a 32-bit linear address from the TBC to a segment and an offset.

Because the TBC has a larger addressing range than the 80186, you can locate the TBC's 128-byte private area of RAM beyond the addressing range of the 80186, but within the range of the TBC. This isolates the private area from the μP and any intrusive software, and it also ensures proper IEEE-802.4 operation.

The interrupt handler for the TBC is defined as a C function, which is addressed at the location for the INT0 autovector (30 hex). At boot-up, the software copies the handler from the EPROM into RAM and substitutes the IRET instruction for the RET instruction, which the C compiler places at the end of the function. The internal 80186 registers map into the memory space, which allows the user to write high-level code to process interrupts like the end-of-interrupt (EOI) instruction. The EOI instruction is necessary to clear the in-service bit for the particular

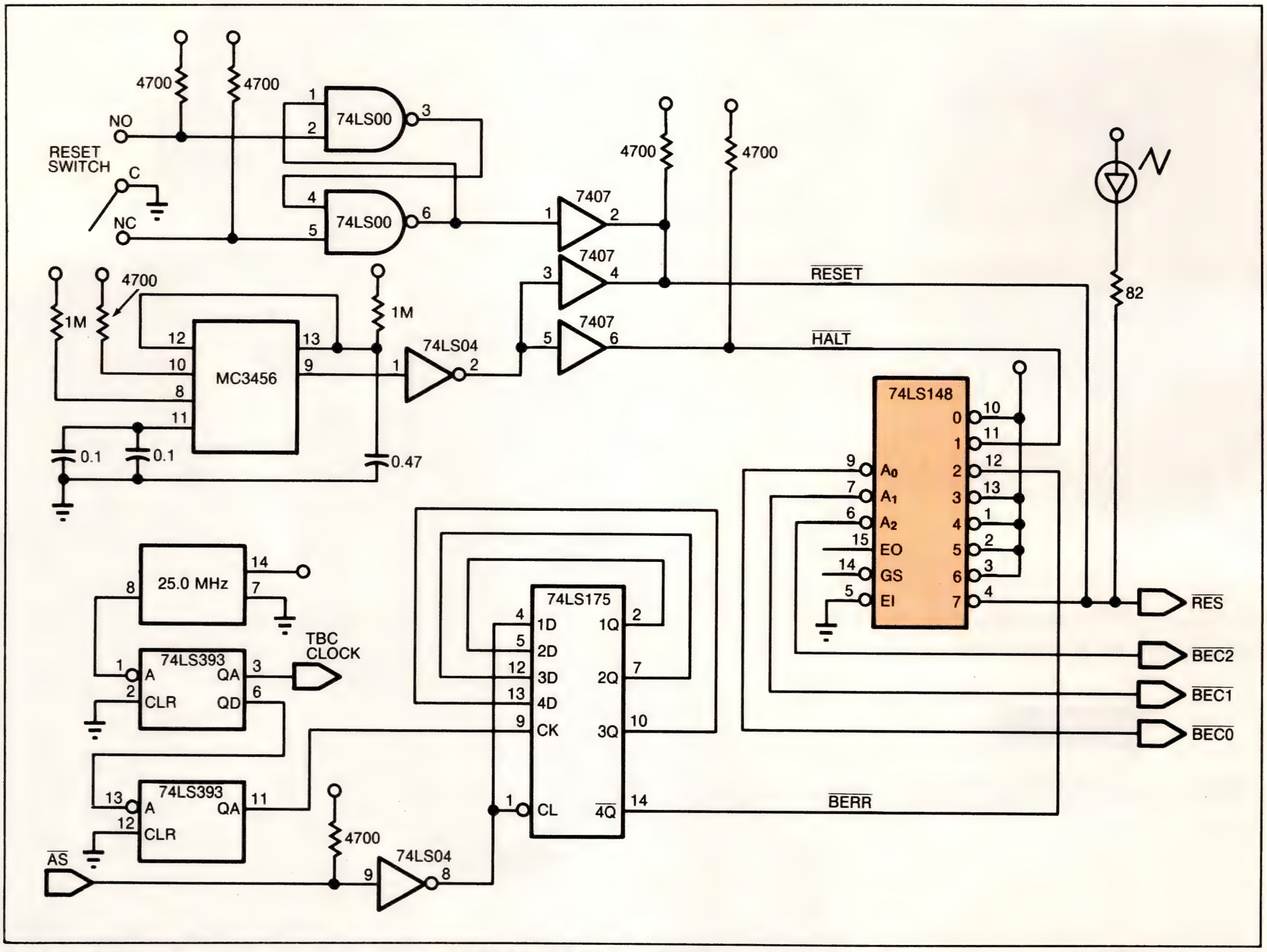

***Fig 9—A 74LS148 priority encoder translates** the $\overline{RESET}$, $\overline{HALT}$, and $\overline{BERR}$ signals to bus exception conditions on the $\overline{BEC}_{0\text{-}2}$ lines to the TBC.*

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interrupt being serviced. The handler monitors both of the TBC's interrupt status words and responds to any bits that are set.

When designing a token bus interface, you should have overall system performance objectives in mind, which requires a thorough calculation of the expected network data rate in bytes/sec and the number of stations on the network, as well as system parameters like memory cycle time and arbitration latency. A good TBC interface should not occupy much more than 15% of the overall system bandwidth. If the interface design significantly exceeds this value, you should increase the system resources available to the TBC or host. These include such factors as faster clock speeds and faster memory chips. In addition, the TBC should be given a high priority on the local bus because of the real-time nature of the token bus medium. The system should only allocate dynamic-RAM refreshes at a higher priority than the TBC. **EDN**

Reference

1. Ivan Erickson, "Token-ring bus controller simplifies network design," *EDN*, April 30, 1987, pg 159.

Author's biography

Paul Polansky is an applications engineer at Motorola's High End Microprocessor Div in Austin, Texas. He holds BSEE and MBA degrees from the University of Texas in Austin. Paul is a member of the American Finance Association and enjoys racquetball, weightlifting, backpacking, and movies in his spare time.

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Evaluate model types before simulating logic circuits

By modeling your logic-circuit design in software before, or in place of, building a hardware prototype, you can save yourself a great deal of time and money. Before you can make this determination, however, you must know more about the four basic types of simulation models.

Kent Moffat and Don Carter,
Mentor Graphics Corp

It is well known that you can avoid the expense of fabricating a flawed circuit or system by first "building" and testing a model of the device. However, there are several very different types of models you can choose from, and you'll find that some designs call for the use of multiple model types. Before you start developing a simulation strategy, you should carefully consider each type of model. The model or models you select will determine your simulation's speed, accuracy, and the number of reports that it produces. By choosing carefully, you can meet all of your requirements.

Models are principally classed according to whether they are software or hardware based (**Fig 1**). You'll find advantages and disadvantages to both of these approaches. For example, you can construct a software simulation model in the same amount of time—or less—than it takes to construct a complete prototype circuit or system (see **box,** "Software breadboard reduces required investment"). And, once you have such a model, you can debug and correct it quickly. Because it takes more time to physically test and rewire a hardware prototype, the design-verification costs for software models are often lower.

On the other hand, hardware models use a real IC, and thus they provide all of the good—and the faulty—functions of a chip. A software model is only as accurate as the tests written to verify its operation; it is almost impossible for a software model to simulate both the good and faulty functions of a device. For example, a software model probably won't contain a response for each illegal input-signal combination that you can possibly apply to a µP chip. Likewise, it's unlikely that a chip's undocumented features and bugs are available in a software model, unless the model's programmer had access to the chip maker's proprietary information. You can see that you must thoroughly understand and carefully weigh your simulation requirements against the relative benefits and drawbacks of the two disciplines.

Software models are further categorized according to the complexity level of the devices they effectively

All but the simplest logic circuits can benefit from simulation techniques.

simulate. Gate-level models, for example, are software models that simulate primitive logic devices such as individual AND, NAND, and OR gates by exactly describing each gate's internal logic. These models are useful in describing individual gates that aren't part of a large chip (**Fig 2**).

On the down side, gate-level models require a good deal of time to develop. Also, because the simulation software must evaluate each gate's response to every simulation event, simulation run-times are lengthy as well. Even a gate-level simulation of the devices on one pc board, such as a VME Bus CPU board, consumes more computer time than is practical. Gate-level accelerators can help speed this type of simulation, but they are expensive and inflexible.

Likewise, because gate-level models must duplicate each gate in a chip's internal circuitry, they are a poor choice for simulating complex ICs. For instance, you can use a manufacturer's spec sheet to find the overall input-to-output signal delay for an IC, but the data sheet won't provide the delay for each of the IC's internal gates. So, if you simply estimate the gate-delay times and then simulate a complex device, timing errors will accumulate and produce erroneous results. Keep in mind, too, that you can't obtain gate-level designs for many proprietary chips. Therefore, gate-level models are appropriate only for small-scale integration (SSI) and medium-scale integration (MSI) ICs.

The next level of software model is the functional model. A functional model uses a simplified device description that accurately describes a device's I/O and timing properties, but it doesn't have to describe each gate within a chip. These types of models also require less computer memory—for design storage and recording of simulation details—than gate-level models.

Functional models require a software language that reveals a device's structure. Designers typically construct these models by connecting simulation primitives such as gates, registers, and other common logic functions:

```
SUM ≤ X xor Y xor CIN after 5 ns;
C ≤ (Y and CIN) or (X and CIN) or (X and Y);
COUT ≤ C after 6 ns
```

For functional modeling, you can also express a device's function in a Boolean language. For example, Mentor Graphics' functional-modeling language lets you create a schematic that is made up of primitives that model a device's operation. You combine this schematic with a text file that describes the device's input-to-output, or pin-to-pin, timing relationships.

Functional-model libraries include most MSI and some LSI ICs. But, if you can't find a needed functional model in a library, you can create it yourself. For instance, you can model an address latch by describing the device's logic and by entering the data sheet's timing information.

Although functional models work well for MSI chips, you can't use them to describe VLSI (very large scale integrated) components. Functional models simply interconnect logical elements, and it's inefficient—and often impossible—to use them to describe a VLSI device. Therefore, to model all VLSI and most LSI devices, you must use a behavioral-modeling language. Such languages use a series of instructions and equa-

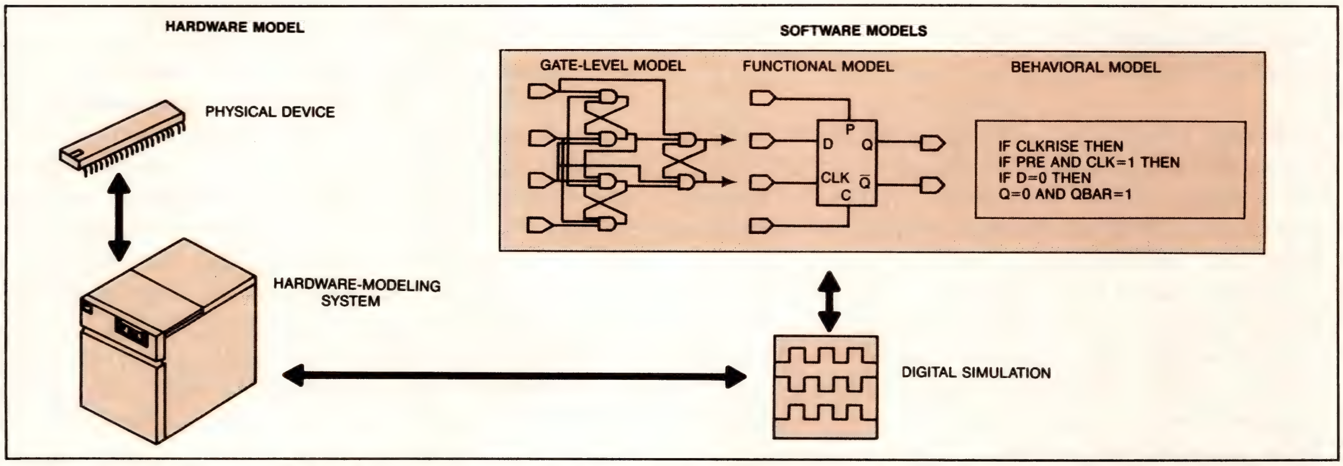

Fig 1—Simulating a complex digital circuit *may require all four types of models: gate-level, functional, behavioral, and hardware. Specific choices depend on the complexity of your design.*

tions to describe a device's timing and logic.

In contrast to functional languages, behavioral languages do not describe a device's structure in terms of existing simulation models or primitives. Instead, they use languages similar to C and Pascal. In fact, several CAE systems use an extended form of C or Pascal as their behavioral-modeling language:

```
while (TX < TY)
  loop
    TX := TX + 1;
    TSUM := TSUM * TX;
  end loop;
```

In general, behavioral languages are more flexible and can describe more complex devices than functional languages. ASICs are typical of devices that you would model with a behavioral-modeling language. Because each ASIC is unique, ASIC models aren't available in a standard-device library.

The VHSIC Description Language (VHDL), an emerging IEEE standard, includes both functional- and behavioral-modeling constructs. You can therefore use each modeling method to its best advantage. Both of the previously shown functional- and behaviorial-program examples conform to this IEEE specification.

Microprocessors and other standard VLSI devices also benefit from behavioral models. A μP gate-level simulation takes months to develop, consumes large amounts of memory, and delivers inaccurate results due to timing errors. Moreover, behavioral models let you simulate VLSI devices that aren't yet available.

Behavioral-modeling languages also give you better control of your simulations. You can augment a behavioral model by adding to the software several design and debugging aids to produce error messages, perform timing checks, and issue instructions to device handlers. And, you can trade detailed reporting for speed, programming your model to simulate only the modes that your design uses and to leave out report-generating steps.

Use ready-made models

For all their flexibility, behavioral models do have a disadvantage; it takes a great deal of time to write them—often several months. However, you can purchase models of many standard VLSI components from vendors such as Mentor Graphics or from model vendors such as Logic Automation (Beaverton, OR) and Quadtree (Bridgewater, NJ). For complex components such as floating-point arithmetic-logic units, a commercial behavioral model is a good choice.

Behavioral-model vendors offer two types of models. The first of these is the full-functional model, which simulates the complete instruction sets and timing characteristics of complex chips such as μPs. These models simulate the execution of a μP's individual op codes. The second model is the bus-functional model, which simulates only bus operations and bus-timing cycles. If you're using a simulation to test a μP's microcode, you can't use a bus-functional model because it doesn't contain the information that characterizes each of the μP's op codes.

A processor-control-language (PCL) file controls bus-functional models. These PCL files are relatively easy

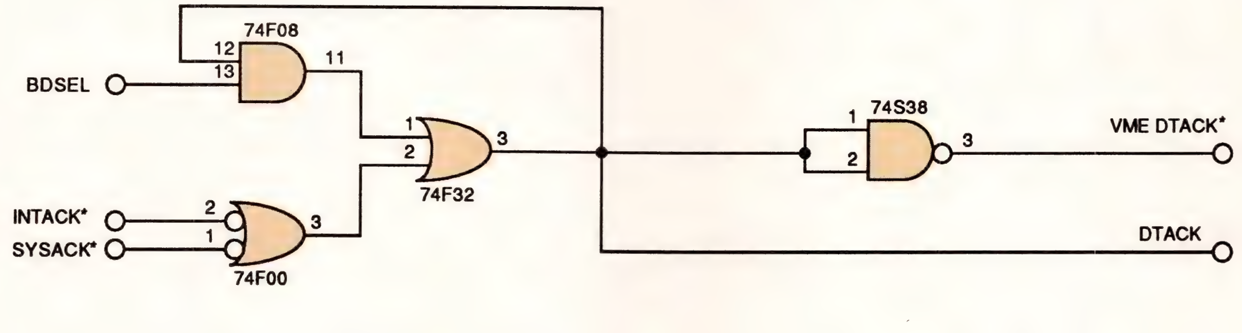

Fig 2—You can use gate-level simulation *when individual logic circuits don't fit within the architecture of larger devices. Control circuits that require SSI chips are candidates for gate-level simulations.*

Gate-level simulation works well for SSI components, but it requires extra preprocessing time.

to develop. For example, a PCL file that simulates a 68020 μP's write-memory and read-memory cycles requires only five statements:

```
processor MC68020
   begin
      write 5,16#620,4,16#FFFF
      read 5,16#624,4,16#AAAA
   end
```

Although a detailed description of the program lines is beyond this article's scope, it should be evident that it's possible to simulate a complex operation in software.

Commercial behavioral models provide features that help you evaluate your system and improve your design. Models can not only identify timing errors for you, but can also help explain them. You can also write behavioral models to tell you of errors such as those that involve the misuse of a μP's internal registers. These error-handling techniques can dramatically improve your debugging efficiency. Commercial models sometimes offer a choice of clock frequencies and timing delays for the devices they simulate.

Hardware models are most accurate

The fourth type of device model—the hardware model—is the most accurate. Although software and hardware models basically operate in the same way, hardware models are incapable of making interpretation errors because they derive responses directly from a real device and not from a group of simulation instructions. Furthermore, software models must acquire timing information from a look-up file. Hardware models, in contrast, can obtain timing information from an attached timing analyzer that measures delays directly from device responses. By using a timing analyzer, you can avoid developing a timing shell for your IC.

Hardware models run quickly, so you can use them to simulate several ASICs. Thus, by plugging a prototype of a bus-controller gate-array IC into a hardware-modeling system, you can simulate your VME Bus CPU board much faster than would be possible with a gate-level model. And, in addition to running your simulation faster, hardware modeling also lets you evaluate the ASIC prototype chip.

Hardware models do have limits

Hardware-modeling systems also have their drawbacks, however. You can't use a hardware-modeling system unless its speed, memory capacity, and available pin count are adequate for your application. As an example, Mentor Graphic's Hardware Modeling Library operates at 16 MHz, controls a maximum of 256 pins on each device, and stores as many as 256,000 stimulus vectors for each pin. A model built completely of software commands doesn't have such limitations. Because software models don't physically exist as wires and circuits, you can program them to run at almost any speed. You simply tell the software model how fast you

Software breadboard reduces required investment

To use a software simulation technique effectively, you first "capture" your schematic by using a computer or workstation to retrieve components from simulation libraries. The investment required to build this "software breadboard" is much less than that required to build a traditional breadboard. Also, as far as you're concerned, the software model will function in the same manner as the breadboarded circuit.

To simulate a digital system, for example, you need a simulation program, a computer or workstation, and models of your system's digital components. The models exist as software statements that duplicate the digital circuits' operation.

Once you've captured the design, simulation can begin. Workstations such as Mentor Graphic's QuickSim provide the input signals that drive your design. Obviously, the simulation doesn't involve real stimulus signals. Instead, software operations control the simulation and graphically display signal waveforms just as you'd see them on a logic analyzer.

Also, you can place software probes in the schematic just as you would connect logic-analyzer probes to your circuit breadboard. When errors are found during simulation, you can then revise your schematic and resimulate the circuit. This approach is usually faster than rewiring a breadboard and retesting your circuit.

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Hardware models let you obtain simulation data directly from ASICs and other complex ICs.

want the simulated signals to operate when you run the simulation on your CAE workstation.

Also, hardware-modeling systems require a sizable investment in equipment. Depending on a hardware-modeling system's operating speed, its ability to handle multiple users, and the number of models in its library, it can cost $40,000 to $90,000. Thus, the choice between a hardware-modeling system and commercial behavioral models depends on the number of devices that you're modeling and the number of simulations that you'll be performing. The more models you need, the more cost effective hardware modeling becomes. Also, one hardware-modeling system can typically serve a network of users.

There are other considerations, too

After you determine which types of models you'll need, the availability of accurate models must be your next concern. If you don't have a working version of your ASIC or other IC, for example, you can't use a hardware model to simulate it. Model availability is even more of a problem for software models than for hardware models. Commercial behavioral models of many VLSI components just aren't available. Even among the available models, most are bus-functional, not full-functional, models.

You can create a hardware model and testing information for a typical VLSI component in about a month, and with a bit of experience, you can reduce this time to two to three weeks. In contrast, you need between six months and a year to write a behavioral model for the same device. Before you select a model, make sure it is available and that it provides all the functions you need.

Don't forget to also consider the time available on your computer system for modeling programs. Especially for short simulation runs, preprocessing time can play a major role in determining a simulation's length (see **box,** "Allow time for preprocessing"). Keep in mind that hardware models require less preprocessing time than any type of software model.

Multiple simulations and system-level modeling

For some advanced applications, you can improve the quality of your analysis by swapping different types of models and then repeating a simulation. During each simulation, you adjust and improve your models for increased accuracy and performance, until you are satisfied with the results.

Architectural-level simulations of entire systems can also benefit from model swapping. You start your simulation at the architectural level by writing behavioral models of large system blocks. Once you verify the proper operation of the blocks, you replace each block with the interconnected components that each contains.

For a system that runs microcode, you can begin analyzing your system by emulating a representative set of the microcode instructions. Then you can simulate the system's execution of complete instruction words. Your behavioral models record timing results and collect functional statistics as the simulations run.

Allow time for preprocessing

When you evaluate a model's performance, you must consider the simulation's actual run-time as well as its preprocessing time. Both of these factors contribute to the total simulation time. During preprocessing, the simulation software converts your schematic diagram into a simulation file. In creating this file, the preprocessor replaces gate or functional models with primitive library definitions and replaces behavioral models with instructions, logical expressions, and equations. Complex devices require longer preprocessing times than simple ones.

Basically, functional models require less preprocessing time than gate-level models because functional models contain only a few library definitions. Therefore, even though hardware accelerators can speed gate-level logic simulations, this increase in speed is often offset by the additional time needed to preprocess gate-level simulations.

Behavioral models can also be preprocessed in less time than gate-level models because behavioral models have few interconnections. Preprocessing a behavioral model consists primarily of compiling the model's source code into an executable format that runs efficiently. In contrast, hardware models don't have coded definitions at all—the simulator applies stimulus vectors directly to the device. As a result, hardware models have the shortest preprocessing times.

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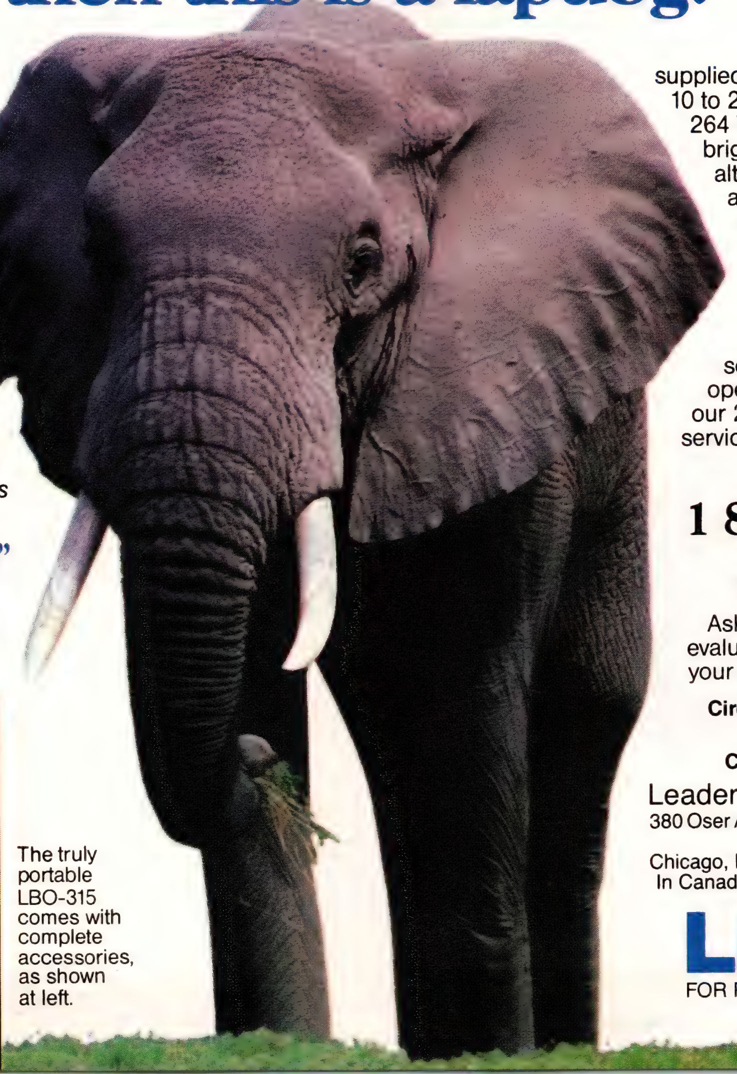

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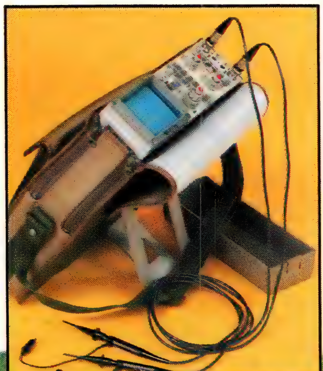

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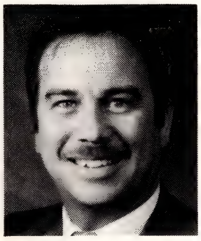
By choosing the optimal type of model for each component in a system simulation, you can verify your design with speed and accuracy. Even though you may need to use different types of models—perhaps all four—you generally need only one of each model to simulate a complete system-level design. **EDN**

Authors' biographies

Kent Moffat is a technical marketing engineer at Mentor Graphics (Beaverton, OR). His job responsibilities include managing the company's parts-library products, developing modeling programs, and defining software requirements. Kent has a BSEE from Stanford University as well as a BA in physics from Willamette University.



Don Carter has worked for Mentor Graphics for six years, and he is now a marketing manager in the company's Major Accounts Div. While at Stanford University as a research associate, Don assisted in the initial development of a microelectronic artificial-hearing implant for the deaf.

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CIRCLE NO 93

DESIGN IDEAS

EDITED BY TARLTON FLEMING

Watchdog circuit makes μP fault tolerant

Mario Milberg
CNEA, Buenos Aires, Argentina

The **Fig 1** circuit provides a watchdog function for the 68705R3 μP. The system generates a temporary reset in response to single faults but resets the μP permanently when two consecutive faults occur. You can apply this technique to other processors, and you can make the system tolerate $N-1$ consecutive faults by replacing the flip-flop IC$_{3A}$ with a modulo-N counter.

At power up, R$_3$ and C$_3$ ensure that the flip-flop IC$_{3B}$ is set ($\overline{Q_{D2}}$ low), which holds the μP in reset mode by driving its $\overline{R}$ input low. You must momentarily depress S$_1$ to initiate program execution.

During normal operation, the μP's PA7 output generates 7-μsec pulses at 6-msec intervals. By continually triggering the one-shot IC$_{2A}$, these pulses maintain the flip-flops IC$_{3A}$ and IC$_{3B}$ in the cleared state. A processor malfunction will interrupt the pulses, causing the circuit to generate a brief reset (see waveform H in **Fig 1**) whose duration depends on R$_2$ and C$_2$. The μP immediately regains control.

The appearance of a second fault triggers the alarm and causes the μP reset to remain low; you must then press S$_1$ to restore control to the processor. If a second fault does not occur, the watchdog pulses clear the flip-flop IC$_{3A}$ so that again two consecutive faults must occur to stop the μP. **EDN**

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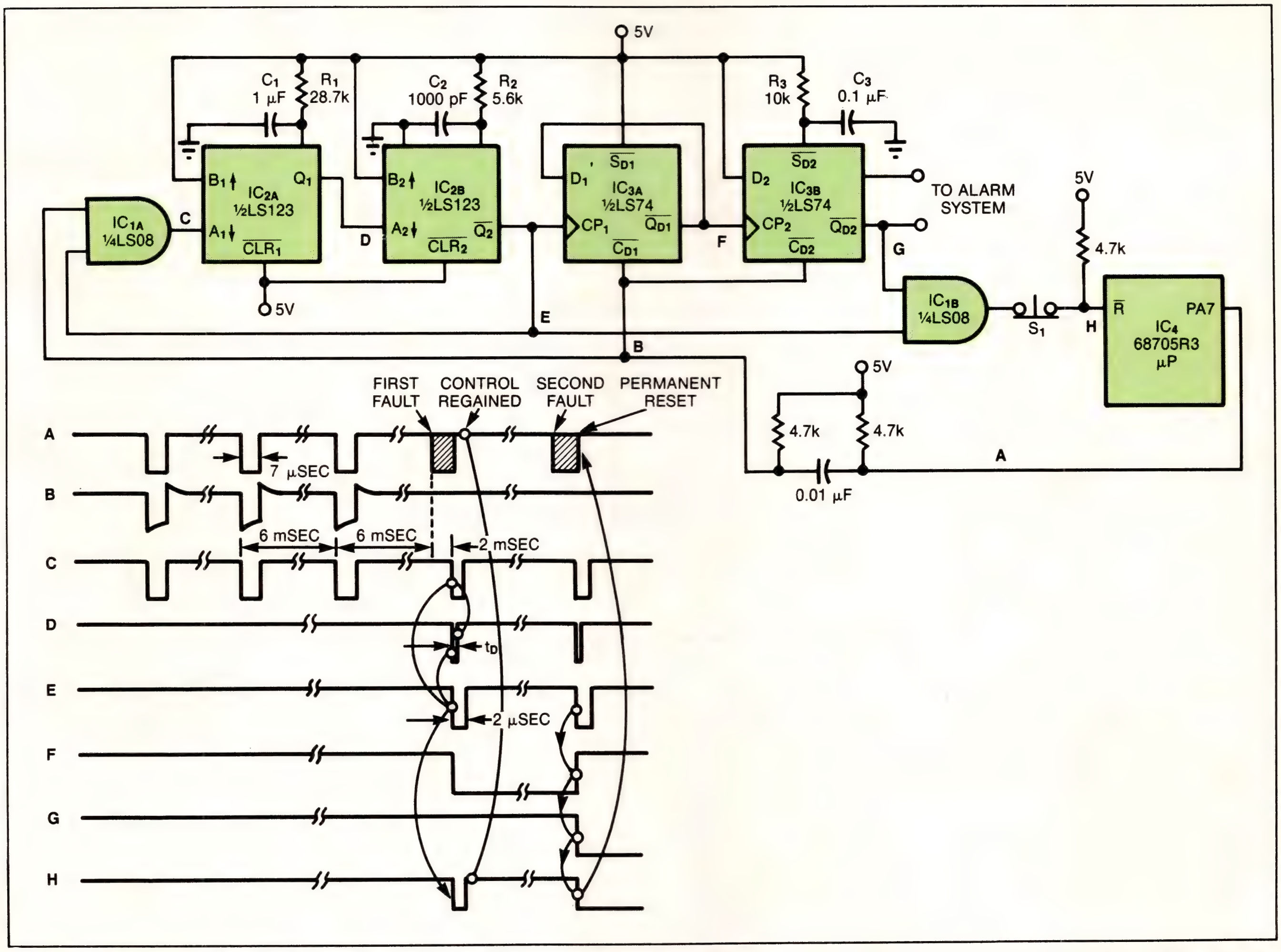

*Fig 1—**This watchdog circuit briefly resets** the μP following a single fault; two consecutive faults reset and halt the μP until you restore operation by pressing S$_1$, a normally closed push button.*

Precision circuit measures shunt resistance

Eric Blomberg
Cogent Design Inc, Brookline, MA

The **Fig 1** circuit allows you to measure unknown resistance values by connecting them in parallel with a known resistance R_T (in this case, a precision 50Ω termination). The circuit is useful, for instance, in trimming resistive RF components that are terminated by a 50Ω precision load.

The DVM (a digital panel meter, for example) measures the voltage V_X produced by forcing a constant 20 mA through the parallel combination of R_T and R_X. V_X is a nonlinear function of R_X, but the DVM's ratiometric property lets you linearize the measurement (**Table 1**) by feeding forward a portion of V_X to the DVM's reference input. (The DVM's ratiometric response is the inverse of the the resistors' proportional current sharing.) A minor modification on the panel meter gives

TABLE 1—REPRESENTATIVE R_X MEASUREMENTS

R_X (Ω)	**R_X/R_T**	**V_X** (V)	**V_{REF}** (V)	**DVM** (COUNT)
80	30.769	0.61538	0.076924	7999
60	27.273	0.54546	0.090908	6000
50	25.000	0.50000	0.100000	5000
40	22.222	0.44444	0.111111	3999
20	14.286	0.28571	0.142858	1999

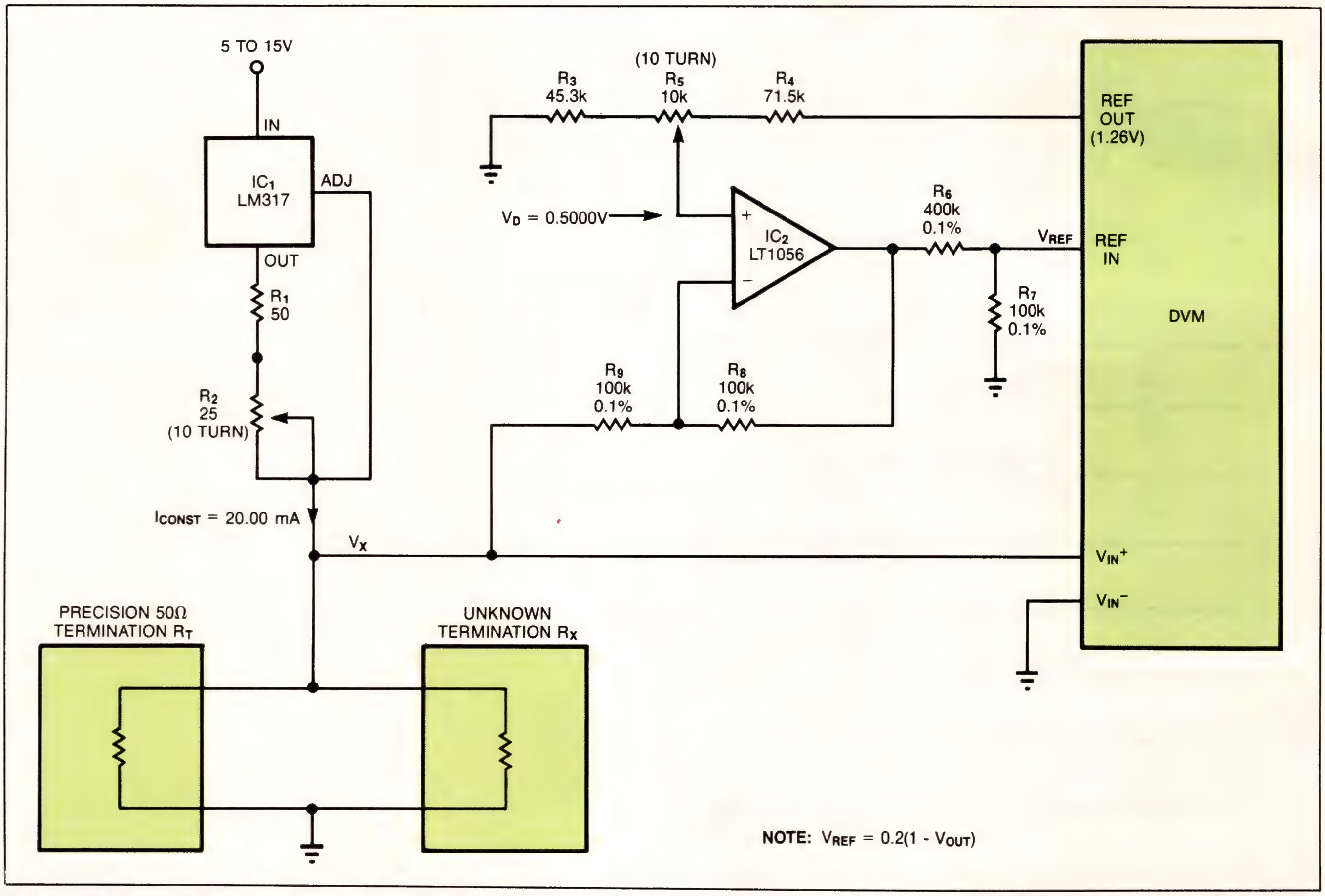

*Fig 1—**This circuit uses a known resistance value** to produce a linear measurement of the unknown value R_X.*

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CIRCLE NO 94

C115 REV. ORIG.

you access to its reference input.

Design equations are

$$V_X = I_{CONST}\left(\frac{R_T R_X}{R_T + R_X}\right)$$

(where I_{CONST} equals 20 mA),

$$V_{REF} = \frac{2V_D - V_X}{5}$$

(where V_D is a constant voltage derived from the DVM's reference voltage), and

$$\text{DVM READING} = 0.1\left(\frac{V_X}{V_{REF}}\right).$$

The values shown provide reliable ±0.1% measurements. To achieve greater precision, you must account for the stability of I_{CONST}, the op amp's input-offset voltage, and the resistor values' tolerances. Note also that the shunting effect of R_9 causes a worst-case error of 0.015% in measuring $R_X=20\Omega$. **EDN**

To Vote For This Design, Circle No 747

Converter output swings 5V using 5V supply

Mike Jachowski
Precision Monolithics Inc, Santa Clara, CA

The **Fig 1** circuit offers a 0 to nearly 5V output swing while operating on a single 5V supply. The 8-bit, CMOS D/A converter (IC_1) behaves like a digital potentiometer by operating in the voltage mode rather than the more conventional current mode. That is, the V_{REF} terminal (pin 15) produces a digitally controlled output voltage when you apply a 1.25V reference voltage to pin 1. The op amp, transistor, and associated components constitute a gain-of-4 amplifier that can swing V_{OUT} to within one $V_{CE(SAT)}$ of the 5V rail. Potentiometer R_6 adjusts the amplifier's gain.

As you increment the D/A converter's input code from $00H_{HEX}$ to FFH_{HEX}, the pin-15 output increases from 0 to 1.25V. Resistor R_2 loads the op amp and draws an output current that also flows in R_1 (along with the op amp's 20-μA quiescent current). When the op-amp output reaches 0.5V, the R_2 current is 50 μA. The resulting 70 μA in R_1 produces a 0.7V drop that begins to turn on Q_1, allowing the transistor to supply current to the load. In turn, V_{OUT} rises to satisfy the requirements of the op amp's feedback loop.

Because the circuit's output drive is the collector of a pnp transistor, V_{OUT} can range as high as 4.97V (with a 5.00V supply and a load of 0.1 to 1.0 mA). V_{OUT} can exceed 4.92V while delivering 10 mA of load current. The circuit, however, consumes less than 120 μA of quiescent supply current when $V_{OUT}=0V$. Quiescent current rises with V_{OUT} because increasing current flows into the base of Q_1; through R_2, R_3, R_4, R_5, and R_6; and into IC_1's pin 1. When the output is delivering 10 mA at 5V, for example, the circuit's quiescent supply current is about 650 μA. **EDN**

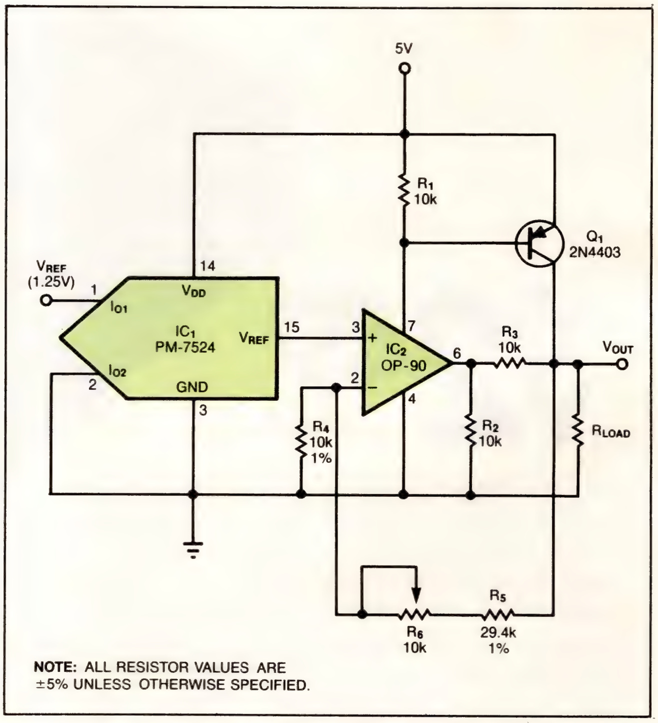

Fig 1—This combination of 8-bit CMOS D/A converter, *low-power op amp, and pnp transistor operates on 5V and produces a digitally controlled 0 to 5V output.*

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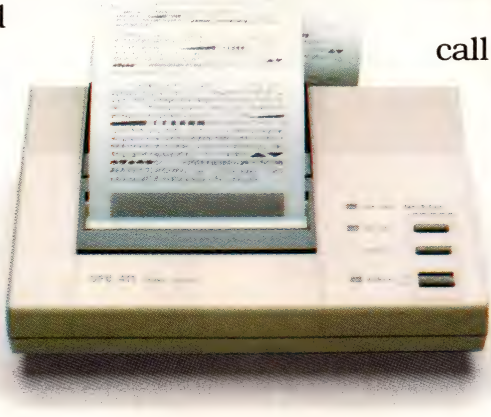

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CIRCLE NO 95

Multidrop circuit cuts cable cost

R Jayapal
Bharat Heavy Electricals Ltd,
Tiruchirapalli, India

The multidrop arrangement in **Fig 1** enables a CPU system to monitor as many as 255 points of contact closure, valve status (open or closed), and other 1-bit data sources. The system minimizes cabling by using a single 3-conductor cable to interconnect the central unit with all field locations.

On command, the system clears all field counters by asserting a momentary high on the PA1 line; it then scans the addresses in ascending order by simply generating a square wave on the clock line. Each field

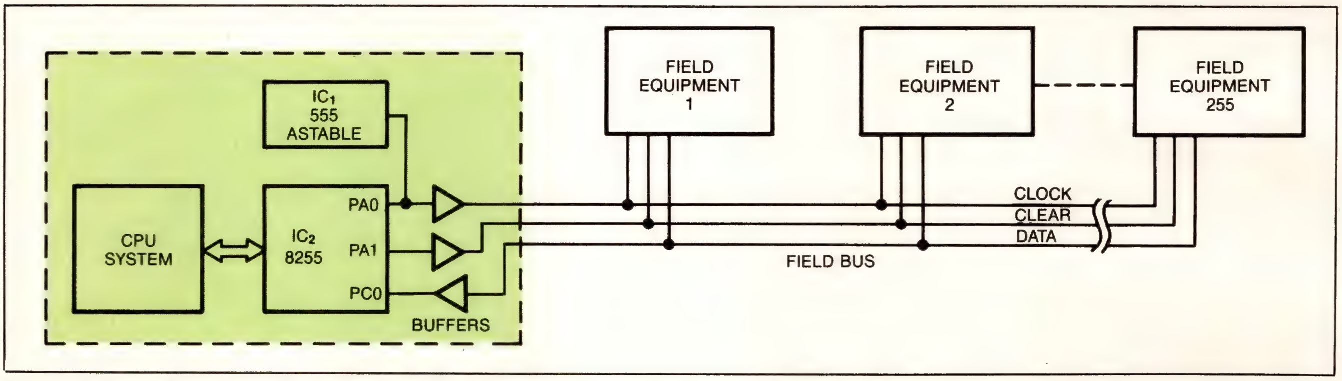

***Fig 1—A single 3-conductor cable** enables this μP system to scan and record as many as 255 single-bit data points.*

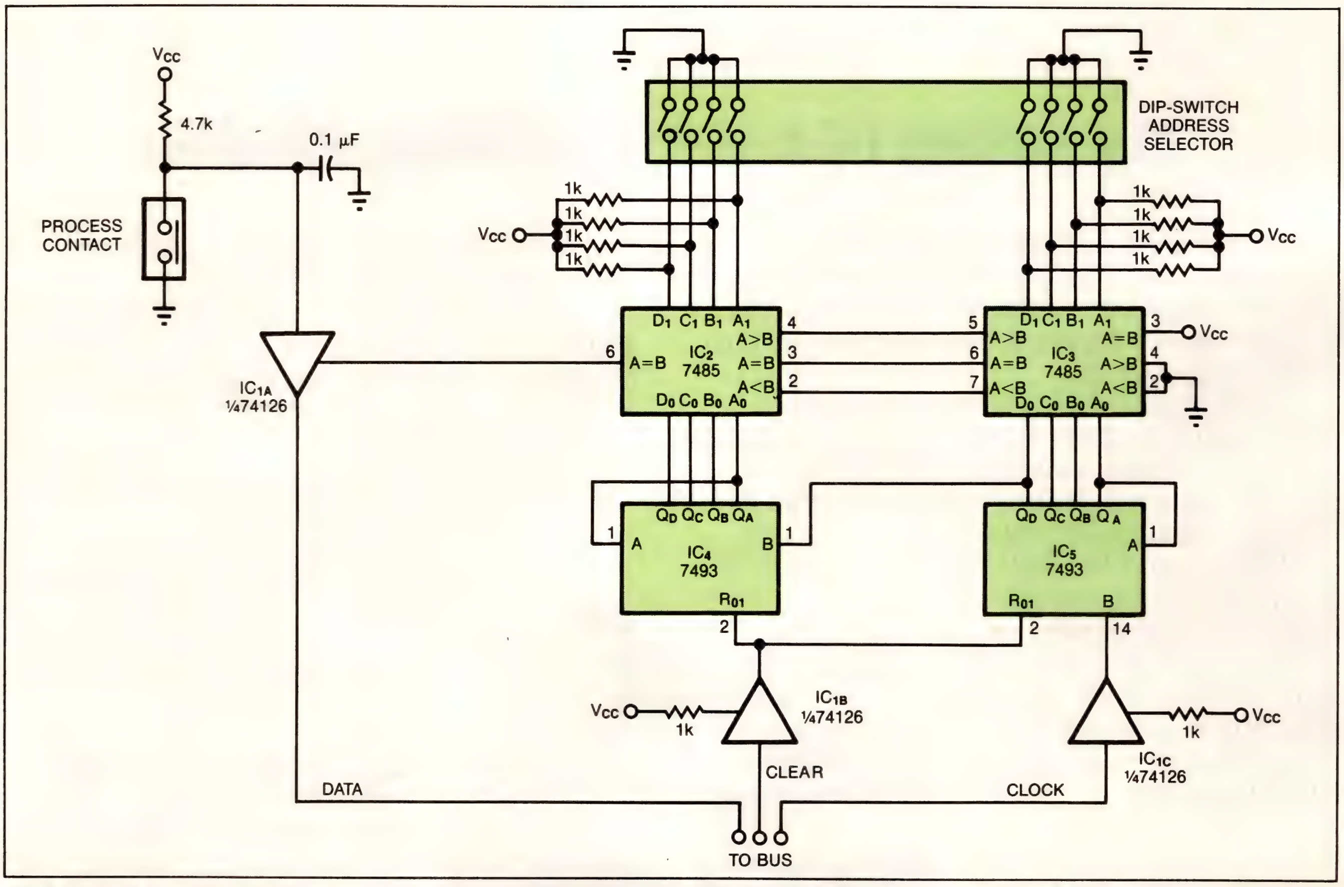

***Fig 2—At a typical field location,** you set the desired address using the DIP switches. The comparators IC_2 and IC_3 then activate the data line only when the counters IC_4 and IC_5 reach that address.*

LINEAR TECHNOLOGY DESIGN NOTES

Number 8 in a series from Linear Technology Corporation *March, 1988*

Inductor Selection for LT1070 Switching Regulators

Jim Williams

A common problem area in switching regulator design is the inductor, and the most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions current flow is limited only by the inductor's DC copper resistance and the source capacity. This is why saturation often results in destructive failures.

While saturation is a prime concern, cost, heating, size, availability and desired performance are also significant. Electromagnetic theory, although applicable to these issues, can be confusing, particularly to the non-specialist.

Practically speaking, an empirical approach is often a good way to approach inductor selection. It permits real time analysis under actual circuit operating conditions using the ultimate simulator—a breadboard. If desired, inductor design theory can be used to augment or confirm experimental results.

Figure 1 shows a typical flyback regulator utilizing the LT1070 switching regulator. A simple approach may be employed to determine the appropriate inductor. A very useful tool is the #845 inductor kit* shown in Figure 2. This kit provides a broad range of inductors for evaluation in test circuits such as Figure 1.

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*Available from Pulse Engineering, Inc., P.O. Box 12235, San Diego, CA 92112, 619-268-2400

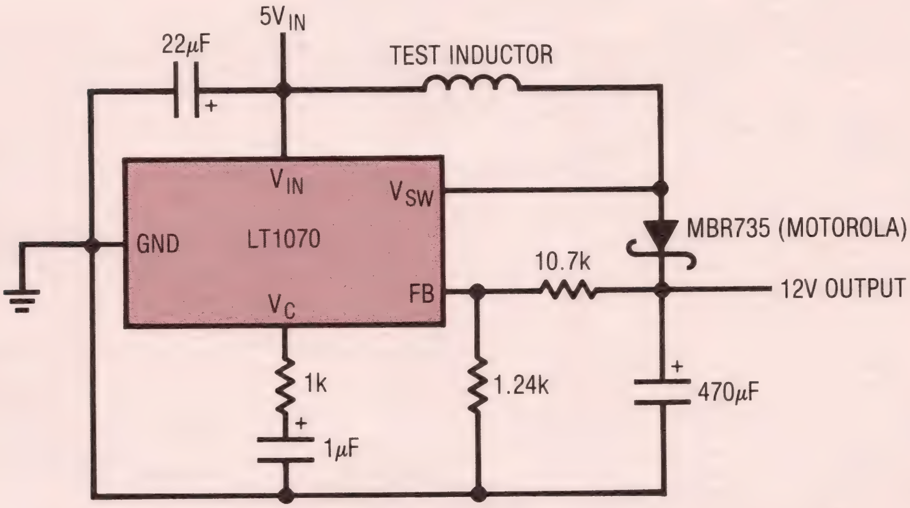

Figure 1. Basic LT1070 Flyback Regulator Test Circuit

Figure 3 was taken with a 450μH value, high core capacity inductor installed. Circuit operating conditions such as input voltage and loading are set at levels appropriate to the intended application. Trace A is the LT1070's V_{SWITCH} pin voltage while trace B shows its current. When V_{SWITCH} pin voltage is low, inductor current flows. The high inductance means current rises relatively slowly, resulting in the shallow slope observed. Behavior is linear, indicating no saturation problems. In Figure 4, a lower value unit with equivalent core characteristics is tried. Current rise is steeper, but saturation is not encountered. Figure 5's selected inductance is still lower, although core characteristics are similar. Here, the current ramp is quite pronounced, but well controlled. Figure 6 brings some informative surprises. This high value unit, wound on a low capacity core, starts out well but heads rapidly into saturation, and is clearly unsuitable.

The described procedure narrows the inductor choice within a range of devices. Several were seen to produce acceptable electrical results, and the "best" unit can be further selected on the basis of cost, size, heating and other parameters. A standard device in the kit may suffice, or a derived version can be supplied by the manufacturer.

Using the standard products in the kit minimizes specification uncertainties, accelerating the dialogue between user and inductor vendor.

References

AN-25 "Switching Regulators for Poets", Jim Williams, Linear Technology Corporation

AN-19 "LT1070 Design Manual", Carl Nelson, Linear Technology Corporation

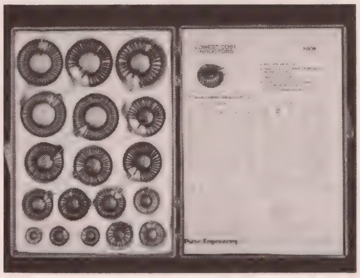

Figure 2. Model 845 Inductor Selection Kit from Pulse Engineering, Inc. (includes 18 fully specified devices)

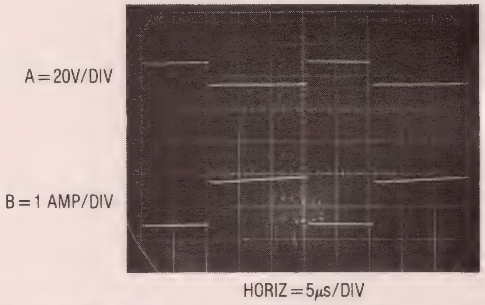

Figure 3. Waveforms for 450μH, High Core Capacity Unit

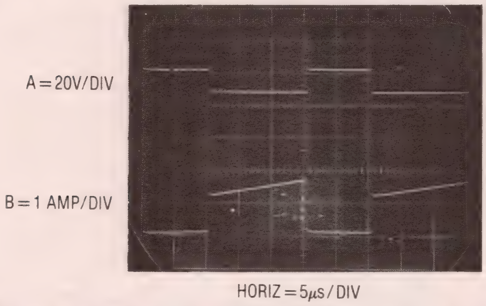

Figure 4. Waveforms for 170μH, High Capacity Core Unit

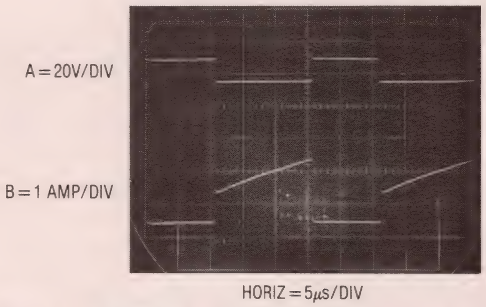

Figure 5. Waveforms for 55μH, High Capacity Core Unit

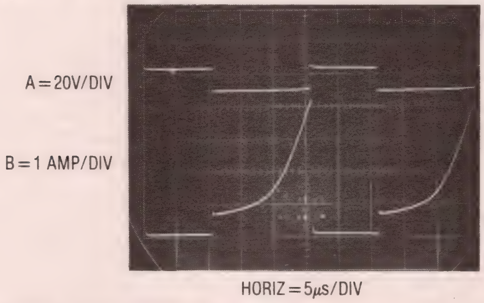

Figure 6. Waveforms for 500μH, Low Capacity Core Inductor (note saturation effects)

For Switching Regulator literature call **800-637-5545**. For help with an application call (408) 432-1900, Ext. 361.

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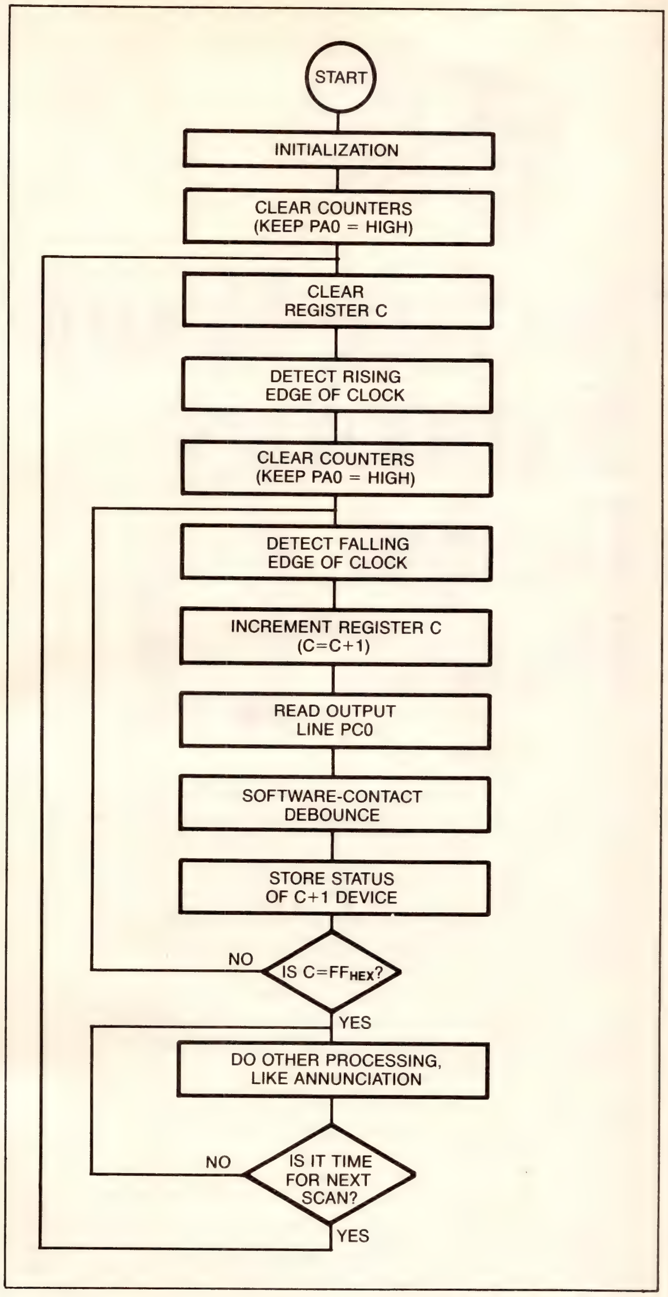
START
INITIALIZATION
CLEAR COUNTERS (KEEP PA0 = HIGH)
CLEAR REGISTER C
DETECT RISING EDGE OF CLOCK
CLEAR COUNTERS (KEEP PA0 = HIGH)
DETECT FALLING EDGE OF CLOCK
INCREMENT REGISTER C (C=C+1)
READ OUTPUT LINE PC0
SOFTWARE-CONTACT DEBOUNCE
STORE STATUS OF C+1 DEVICE
NO
IS C=FF_{HEX}?
YES
DO OTHER PROCESSING, LIKE ANNUNCIATION
NO
IS IT TIME FOR NEXT SCAN?
YES

***Fig 3—Software for the system** shown in **Fig 1** follows this flowchart.*

location (**Fig 2**) includes an 8-bit counter, digital comparator, and DIP switch that enables the location to respond when its counter reaches the address value stored in its DIP switches. The location then responds by asserting its 1-bit data value on the data line; all other data outputs remain in the high-impedance state. The system reads and stores each data point before generating the next address and increments a CPU register to keep track of the address currently active. **Fig 3** is a flow chart for the system's software. **EDN**

To Vote For This Design, Circle No 750

Spy terminal monitors RS-232C traffic

Sebastiao Santiago Barretto
Scopus Tecnologia S A, Sao Paulo, Brazil

Fig 1 shows a simplification of the Design Idea "Line tap aids software debugging" (*EDN*, July 9, 1987, pg 268). Using just two diodes and one resistor, this circuit allows a spy terminal to monitor RS-232C communications between two computers. The circuit also allows you to enter messages on the spy terminal's display via its keyboard.

Current flowing from the spy terminal's output (pin 3) through R_1 maintains the spy-terminal input (pin 2) in a Mark condition (−V) except when data passes between the target and host computers. Then, current flowing through one of the diodes pulls the spy-terminal input to the Space condition (+V). You can use any diode whose reverse-breakdown voltage exceeds 25V. **EDN**

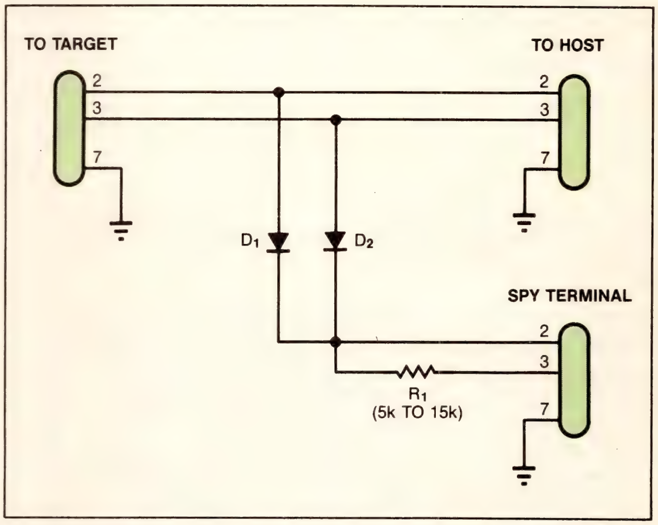

***Fig 1—This simple circuit allows the spy terminal** to monitor RS-232C traffic between the target and host computers.*

To Vote For This Design, Circle No 748

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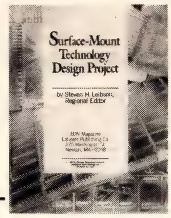

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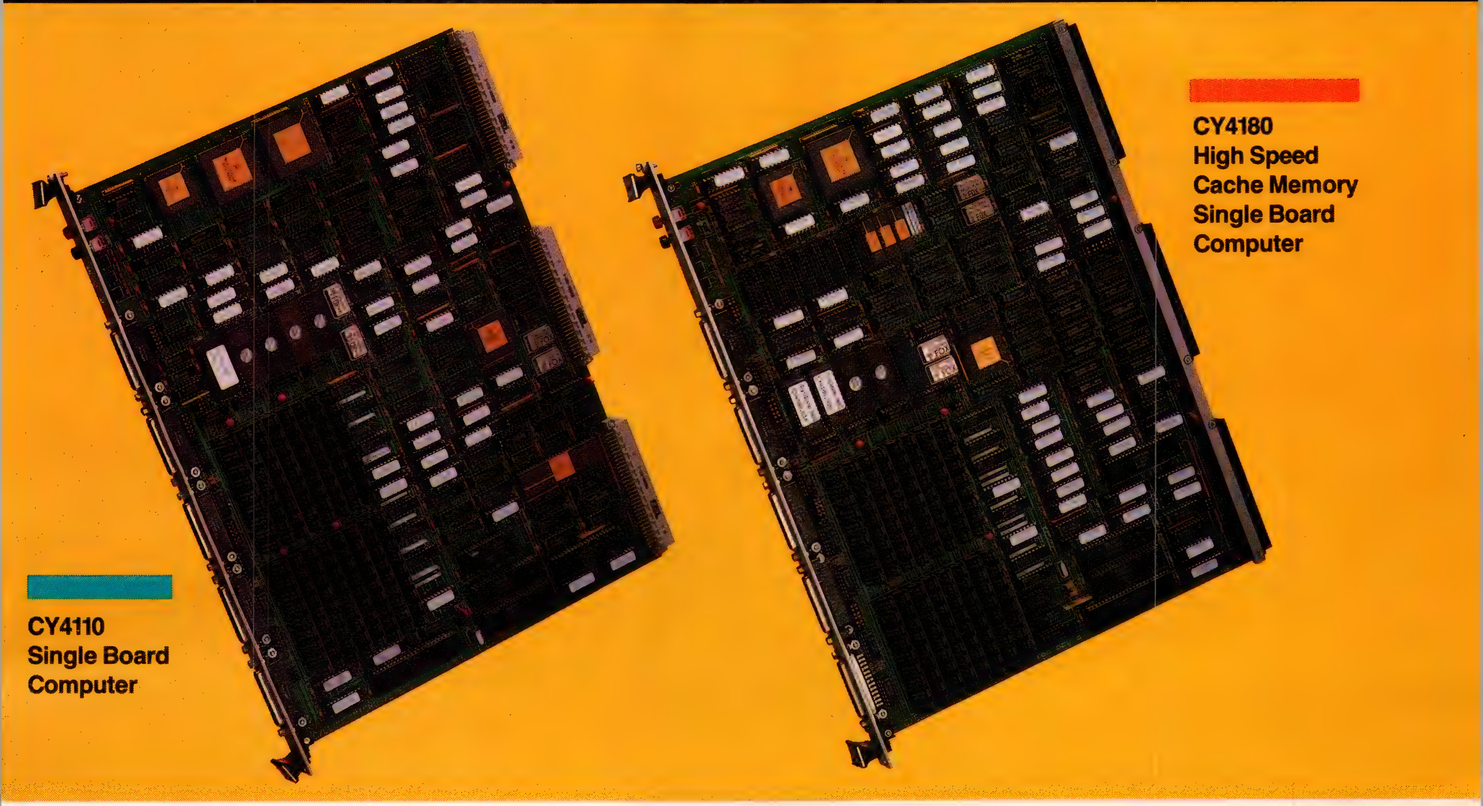

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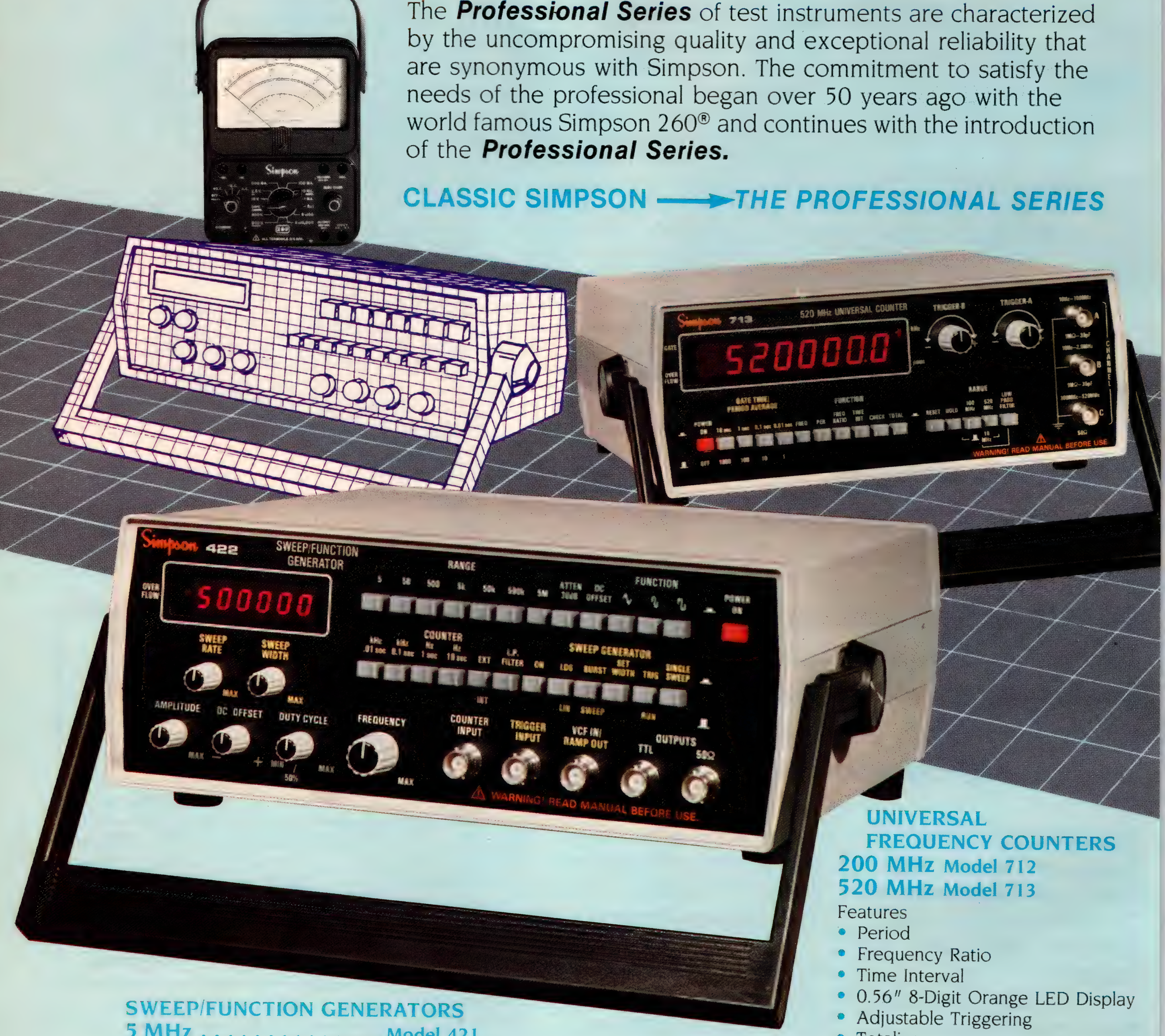

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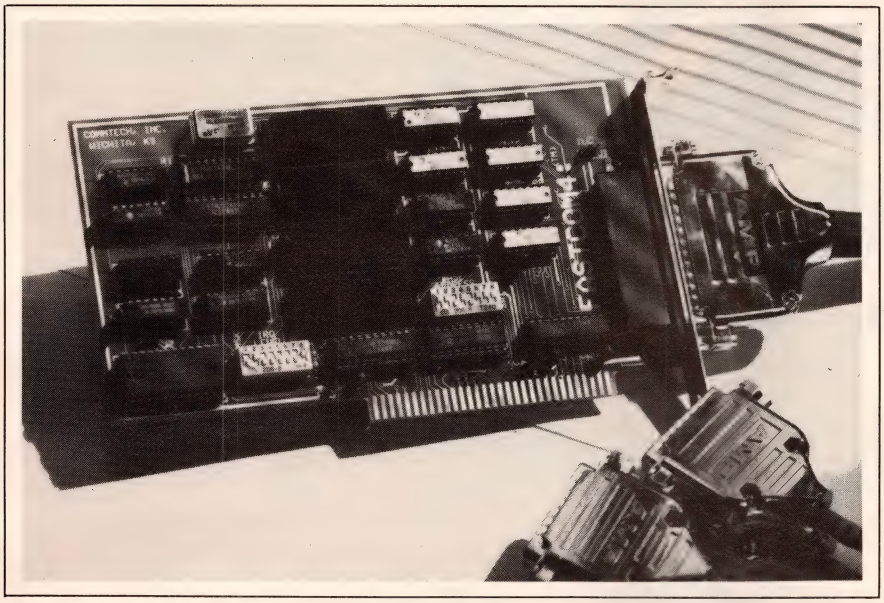


RS-232C ADAPTER

- *Uses the 82050 and the 82510 UARTs*
- *Provides four serial ports for multiple operating systems*

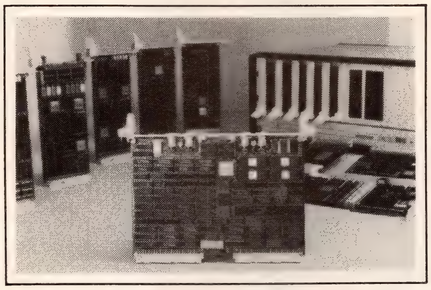
The Fastcom4 communications board for the IBM PC, PC/XT, and PC/AT and compatible computers provides four RS-232C serial ports. The board runs with MS-DOS, Microsoft Xenix, SCO Xenix, and Crosstalk Mk.4. A standard configuration uses Intel's 82050 UART, which is compatible with the 16450 UART but requires less than half the power. The board is optionally available with Intel's 82510 UART, which features two baud-rate generators, a baud-rate range from 50 to 288k baud, and control-character recognition for generating a maskable interrupt. The board comes with cables, RFI shielding, and hardware and software manuals. $375. 82510 UART, $25.

Commtech Inc, 8622 Mt Vernon Ct, Wichita, KS 67207. Phone (316) 651-0077.

Circle No 351

TRANSPUTER BOARD

- *VME Bus board utilizes either a T800 or T414 Transputer*
- *Supports Occam, C, Pascal, and Fortran 77 programs*



The BBK-V2 is a VME Bus processing board. It's equipped with a 20-MHz T800 or T414 Transputer and a 1M- or 2M-byte dual-port RAM that you can access with other VME Bus processors or DMA devices. The onboard Transputer's access to the VME Bus supports A32 and A24 addressing with D32, D16, and D8 Hdata widths. The four Transputer links connect to four communications channels that transmit data at 20M bps. A 1M-byte onboard EPROM also makes the board a stand-alone unit. The double Eurocard board delivers 10 MIPS and 1.5M flops performance figures. The OS-9 and Unix operating systems allow you to use the board as a Transputer development system. The hardware supports the parallel programming language Occam and compilers for C, Pascal, and Fortran 77. DM 8900.

Parsytec GmbH, C&C Marketing, Box 280, Batavia, IL 60510. Phone (312) 879-7003. TLX 4974811.

Circle No 352

GRAPHICS ADAPTER

- *Uses the TMS 34010 as a processor*
- *Provides video capture as well as display*

The NuVista video graphics card for the Macintosh II combines high-resolution video capture and display with a 32-bit, TMS 34010 graphics processor. The board provides capture and display resolutions of 1024×768 pixels; 640×480 pixels; 756×486 pixels; and 738×576 pixels. It features four 8-bit video channels for real-time capture and display. Its 4M bytes of dual-ported video RAM and its video cross-point chip accommodate several memory organizations: 1024×1024 pixels×32 bits, 2048×1024 pixels×16 bits, and 2048×2048 pixels×8 bits. The board produces 16.7 million colors for its RGB outputs. 4M-byte version, $5995; 2M-byte version, $4250.

Truevision Inc, 7351 Shadeland Station, Suite 100, Indianapolis, IN 46256. Phone (317) 841-0332. FAX 317-576-7700.

Circle No 353

MOTION CONTROLLER

- *Controls as many as six axes in a master/slave configuration*
- *Master board has two PWM motor drivers that handle 3A pk*

DRiMotion is a motion controller that can handle as many as six independent axes in a master/slave configuration. A stand-alone master

Conservative thermal design – massive heatsinks and substantial component derating keep temperatures low and reliability high

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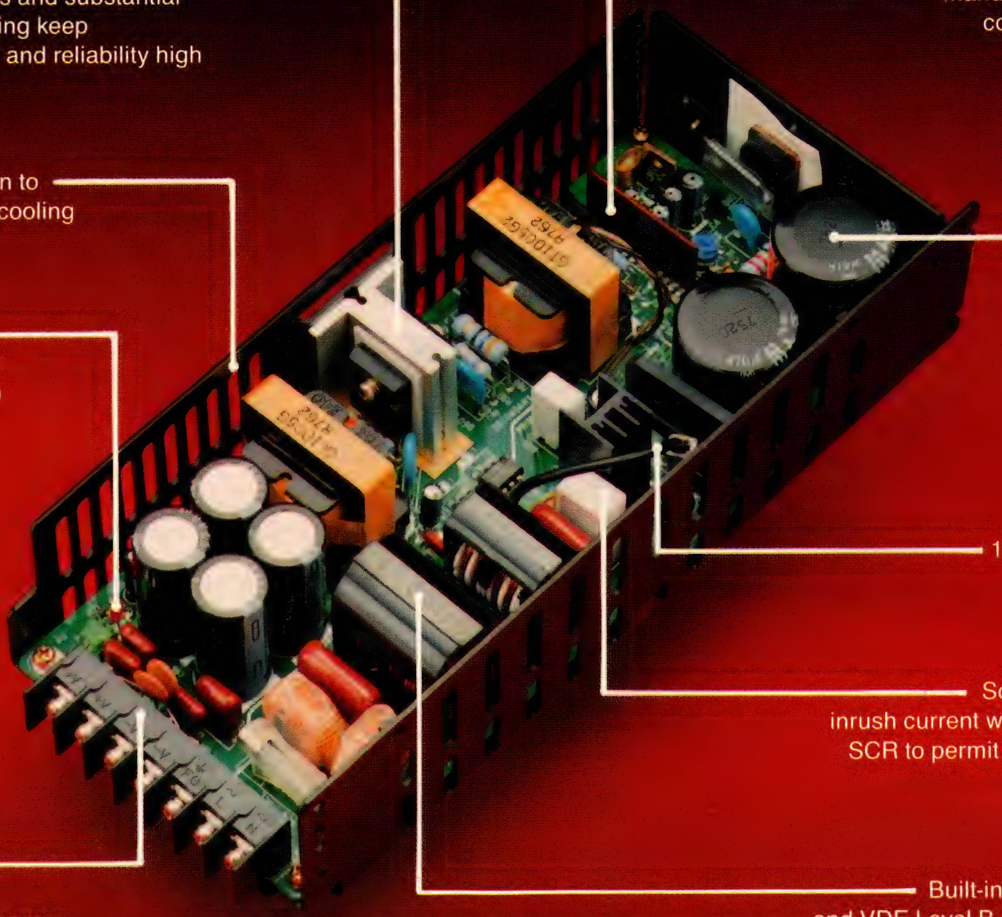

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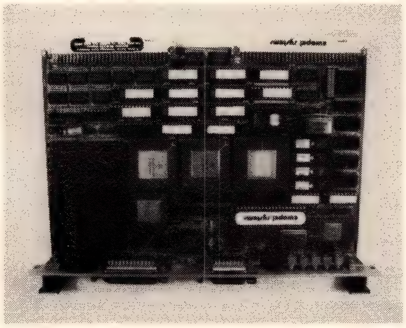
CIRCLE NO 97

board, the MP2, has a 68HC11 microcontroller and two HCTL 1000 motor-controller ICs. The board also contains two PWM motor drivers that can drive 3A max of peak start current; an 8-channel, 8-bit A/D converter; four programmable 8-bit, I/O ports; 16k bytes of EPROM; 32k bytes of static RAM with battery backup; a real-time clock; a UART for communications with a host or modem to 9600 baud; an RS-232C port for communicating with an IBM PC, PC/XT, PC/AT, or compatible computer located as far as 2000m away; and two ports for master/slave communications at a transfer rate of 1M bps. A slave board, the SP1, has one digital motor controller with a PWM driver, an 8-bit µC, 8k bytes of nonvolatile memory, and an 8-channel, 8-bit A/D converter. MP2, $749; SP1, $399.

Dallas Robotics Corp, 1500 E Beltline Rd, Suite 100, Carrollton, TX 75006. Phone (214) 446-2643.

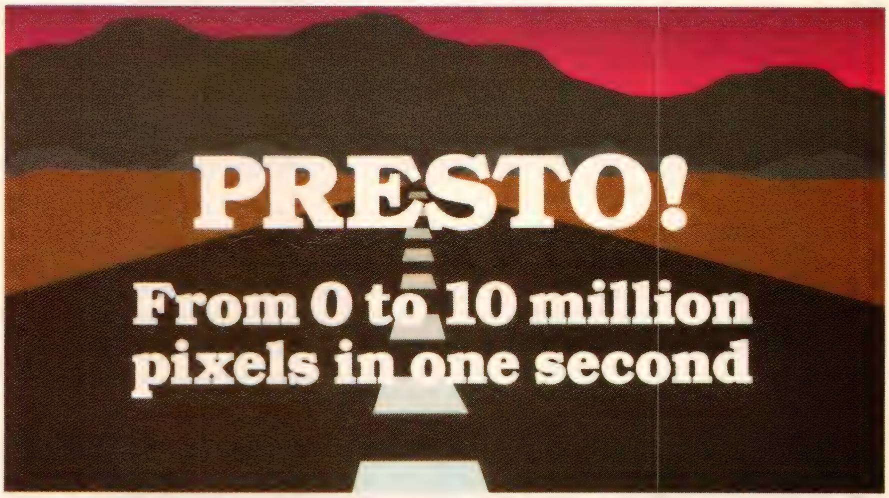
Circle No 354



BOARD COMPUTER

- *Provides a 32-bit Unix workstation on a single VME Bus card*
- *Offloads I/O operations to an onboard IO processor*

The Venus VME Bus-compatible single-board computer has a 68020 µP, 68881 math coprocessor, 68851 paged-memory-management unit, and 4M bytes (16M bytes optional) of RAM. Both the µP and the VME Bus have access to the dual-ported RAM. You can run the Unix System V operating system on the board. To prevent bottlenecks on the main CPU bus, a dedicated I/O processor controls all the board's I/O functions, such as its 1024×768-pixel graphics, audio, and clock/calendar functions, and its SCSI, Ethernet, X.25, keyboard, and mouse interfaces. The boards' VME Bus interface provides AM6/A32/A24 and D32/D16/D8 VME Bus operation in either master or slave modes. The VME Bus interface also includes interrupt-support and system-controller functions. You can order the board as an OEM product with I/O software drivers and a debug monitor, or as a system integration package with a Unix System V license and the Open-Top windowing system. The board is Sun NFS compatible, which permits you to share a


PRESTO!
From 0 to 10 million pixels in one second

Finally a TI™-34010 graphics controller card in sync with your 286/386-based application

Vectrix matches your high-speed microprocessor with high-speed graphics. The PRESTO! graphics controller card utilizes a proprietary Digital Differential Analyzer (DDA), the TI-34010 graphics controller, 512K to 4.5 MBytes of on-board DRAM, and a unique organization of high-speed video shifter RAMS. The result — line drawing speeds in excess of 10 million pixels per second.

5 YEARS OF GRAPHICS EXPERIENCE

Sophisticated technology like this doesn't just happen. Vectrix has been a leader in the complicated and competitive field of graphics for over five years. During that time, we have assembled an experienced, innovative engineering staff ready to focus their expertise on your system needs.

OEM-ORIENTED DEVELOPMENT TOOLS

Because they understand your requirements, our engineers provide a variety of tools to simplify applications development. Onboard high-level graphics commands are accessible directly or through standard programming language libraries provided on disk. Our PRESTO! TI-34010 Toolkit simplifies development of customized firmware. An optional RAM card is available for either data storage or additional code.

PRESTO!'s optional Line Drawing Engine accelerates the speed of the TI-34010. Bitblts, raster ops and enhanced DMA transfer capabilities further enhance PRESTO!'s speed.

Thus PRESTO! is ready to provide the graphics for your next system. And Vectrix stands ready to serve you with state-of-the-art technology, proven product reliability, and an engineering staff capable of translating your system needs into product functionality.

SPECIFICATIONS

Resolution — 1280 x 1024 or 1024 x 768

Available in the following configurations:
16 colors
256 colors from a palette of 4096
256 colors from a palette of 16.8 million

Speed — 10,000,000 pixels per second
  Average Block Move: 25 million bits/second
  Horizontal line or fill: 50 million bits/second
  DMA speed: matches host bus speed

Interface — 16-bit PC family

Video — 60 Hz non-interlaced

SOFTWARE DEVELOPMENT TOOLS

Industry-standard PGL Command Set Compatibility
PRESTO! TI-34010 Developer Toolkit
PRESTO! PGL Developer Toolkit

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CIRCLE NO 100

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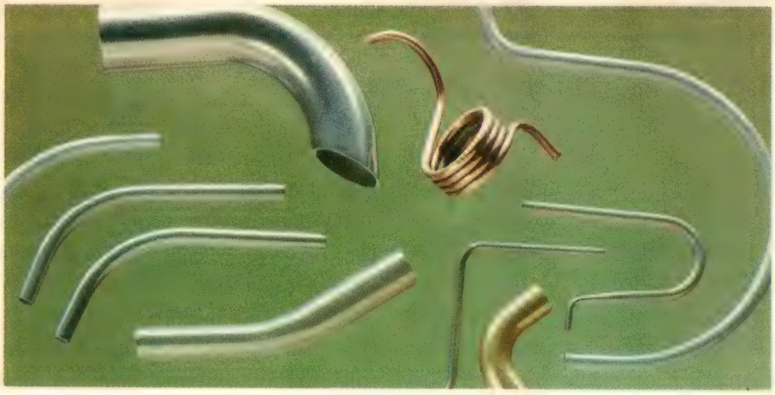

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CIRCLE NO 101

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Model: HC15R5
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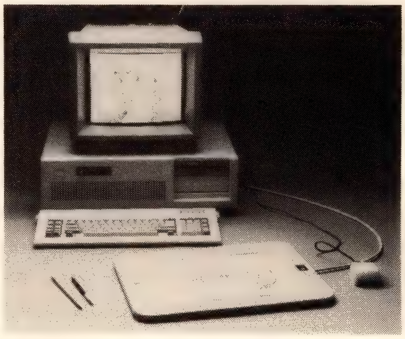
CIRCLE NO 102

virtual file system over a Sun NFS Ethernet LAN. Systems integration package, £4000.

Europel Systems, 5 Vo-Tec Centre, Hambridge Lane, Newbury, Berkshire RG14 5TN, UK. Phone (0635) 31074. TLX 848507.

Circle No 355



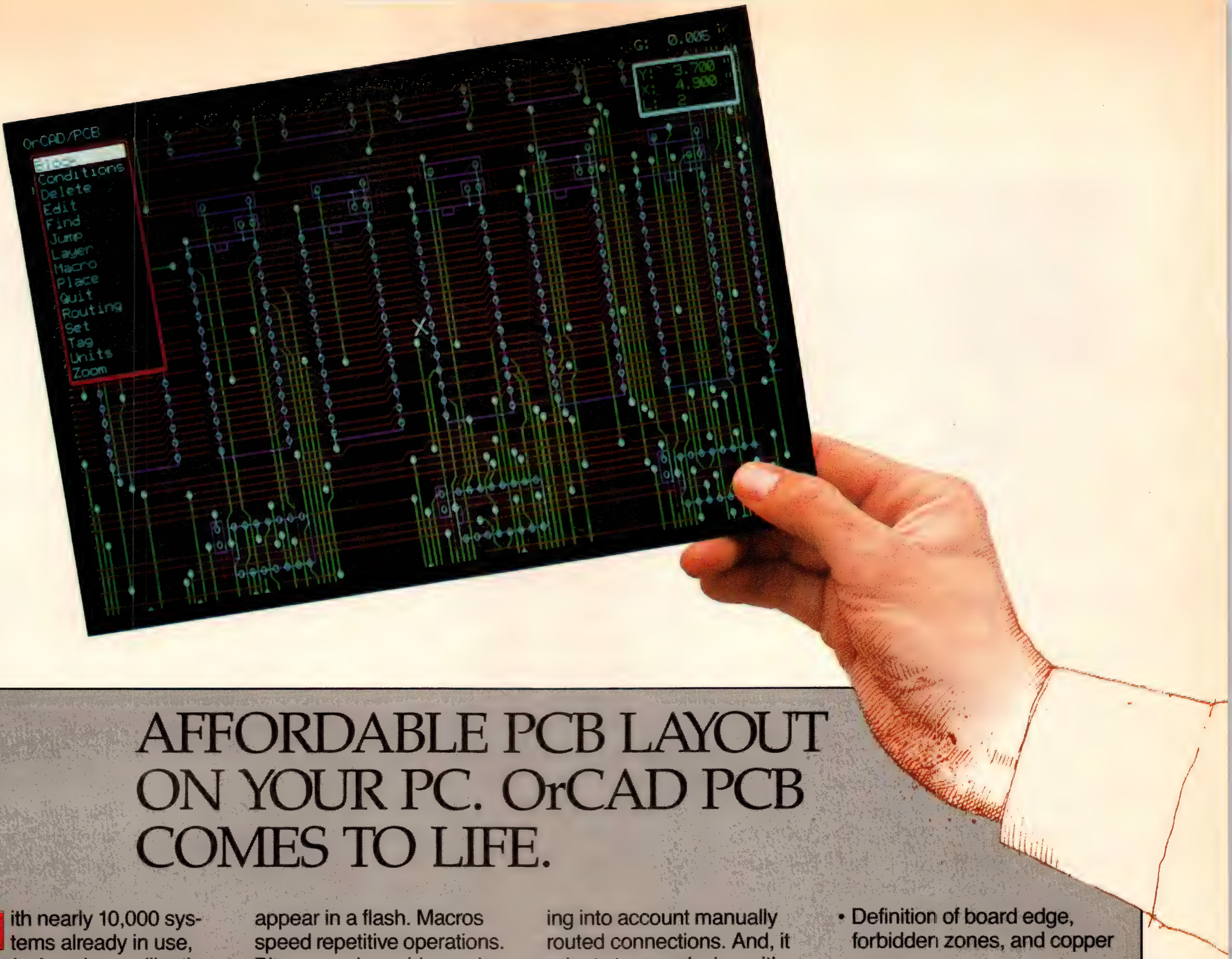
DRAWING TABLET

- *Pressure-sensitive tablet lets you draw into a computer*
- *Plastic material overlays grid of 1024×1024 contacts*

The Easyl PC is a pressure-sensitive tablet that allows you to draw or trace directly into a computer with an ordinary pencil or pen. Its active surface area measures 8.5×12.875 in. and is made of a plastic compound material that overlays a grid of 1024×1024 contact points. The device consists of the tablet and an interface card that occupies one slot of an IBM PC, PC/XT, PC/AT, or a compatible computer, and it sends X and Y coordinate pairs to the computer at rates as high as 200 pairs/sec. The software drivers emulate Summagraphics 961 and Bit Pad 1 standards that allow you to use the tablet with software packages such as PC Paintbrush and Dr Halo in either IBM CGA, EGA, or compatible modes. The package also includes PC Windows and Gem drivers. $539.

Inforite Corp, 1670 S Amphlett Blvd, Suite 201, San Mateo, CA 94402. Phone (415) 571-8766.

Circle No 356



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OR8801-I

CIRCLE NO 103

BUBBLE MEMORY

- *Bubble memory unit runs with STD DOS industrial computers*
- *Removable data cartridge stores 720k bytes of data*

The ZT 8854 is a bubble-memory unit for industrial computer systems running STD DOS. It consists of an electronic drive with a removable cartridge, a disk controller, and an STD DOS software driver. The drive is a functional replacement for 3½-in. half-height drives, and you can plug it directly into an STD Bus card cage. The removable data cartridge stores 720k bytes of data and has an MTBF of 40 years. A design feature of the unit prevents loss of the seed bubble in the chip. An error-detection and error-correction capability, as well as a power-fail circuit increase the unit's reliability. The multiunit disk controller can also interface with two floppy disks and one hard disk while it's controlling the bubble-memory unit. The controller has a SCSI host adapter and provides DMA and interrupt functions. The DOS device driver makes the drive appear as a 720k-byte floppy-disk drive to the STD DOS system. $1800.

Ziatech Corp, 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488.

Circle No 357

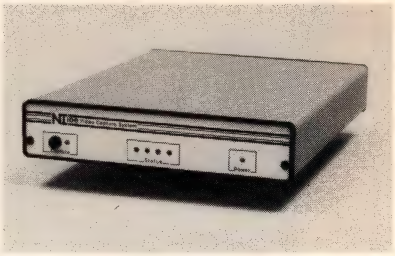

IMAGE DIGITIZER

- *Accepts composite video inputs*
- *Digitizes the image and stores it in 300k bytes of RAM*

The NI-100 Video Capture System is a self-contained image digitizer that operates independent of a host computer. It accepts standard composite video from video cameras and VCRs. The unit uses a flash converter to digitize the image and stores the data in 300k bytes of onboard memory. The host computer accepts the data over an RS-232C or a parallel communications link. The unit grabs real-time frames (1/30

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sec) with 640×480-pixel resolution and 256-level gray scale. Connectors for the RS-170/NTSC input, a monitor output, and computer communications are located on the back panel of a 9×7×1½-in. desktop case. A microcontroller-based design lets you produce custom functions such as data-compression algorithms. $598 (OEM qty).

Lodge Electronics, 1972 Larkin Ave, Elgin, IL 60123. Phone (312) 695-6622.

Circle No 358

LAPTOP COMPUTER

- *Runs on 110V, 220V, a 12V car lighter or a battery pack*
- *LCD backlit screen has 720×350-pixel resolution*

The LP-286 laptop computer is compatible with the IBM PC/AT. It features an 80C286 µP that runs at 6 or 12 MHz with an 80287 coprocessor option. A supertwist backlit LCD screen that is Hercules monochrome compatible provides a resolution of 750×350 pixels. Its 1M byte of RAM memory is expandable to 4M bytes. The unit comes with a 1.44M-byte 3½-in. floppy-disk drive; it has a 20M-byte hard-disk drive with a 65-msec access time. Power for the unit comes from four optional sources: 110V ac, 220V ac, a 12V car lighter, or a battery pack. Two serial ports and one parallel port are also available. A numeric keypad complements the full-sized keyboard. The unit measures 13.6×15×4.2 in. and weighs 15.4 lbs; the battery-pack option increases the weight to 18 lbs. $2495.

Dauphin, 1125 E St Charles Rd, Lombard, IL 60148. Phone (312) 627-4004. TLX 297246.

Circle No 359

I/O CARDS

- *Communicate via a Bitbus network*
- *Suitable for use in harsh industrial environments*

Communicating with a host computer via a Bitbus serial interface, Axiom Bitbus I/O cards allow you to implement distributed I/O applications for industrial automation. The single Eurocard-size cards are available for digital I/O applications, A/D conversion, and D/A conversion. Each card has an onboard 8044/8051

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CIRCLE NO 104

Series microcontroller. You can connect as many as 250 of the interface cards to a single Bitbus network. The DIO 4805 digital interface card provides 48 digital I/O channels that you can select as inputs or outputs in 8-channel groups. The DAD 1612 optically isolated analog-input card has 16 single-ended or 8 differential analog-input channels, and digitizes each channel to 12-bit resolution. Its A/D conversion time is 25 μsec/channel max. The DDA 0812 optically isolated analog-output card provides eight 12-bit-resolution analog outputs that you can jumper-select to operate as analog inputs. Voltage-output or voltage-input ranges are 0 to 10V or −10 to +10V. You can select four of the channels to operate as 0 to 20-mA or 4 to 20-mA current outputs. DIO 4805, DM 1400; DAD 1612, DM 3600; DDA 0812, DM 3500.

Delcon Oy, Lakkisepantie 11, 00621 Helsinki, Finland. Phone (0) 7571744. TLX 123989.

Circle No 360

PORT EXPANDER

- *Drives as many as eight monitors from an IBM PS/2*
- *Supports all four modes of the IBM VGA standard*

The VOPEX-8V is a video port expander for all four PS/2 monitors. The stand-alone unit supports the four modes of IBM VGA operation and drives as many as eight monitors from a single IBM PS/2 or compatible computer located as far as 50 ft away. The unit connects directly to the PS/2's video port via a 4-ft NTI-type cable. It reads the monitor ID code on output port 1 and feeds it to the PS/2 for proper VGA operation. This allows the unit to operate with monochrome and 13- and 14-in. color monitors, as well as with the 16-in. 1024×768-pixel monitor. The unit handles scan rates of 31.5 and 35.5 kHz. Cables with a 15-pin, high-density D connector are available in lengths of 25, 35, and 50 ft. The unit requires 1120V ac and comes in an 8×2.5×6.2-in. chassis. $899.

Network Technologies Inc, 19145 Elizabeth St, Aurora, OH 44202. Phone (216) 543-1646.

Circle No 361

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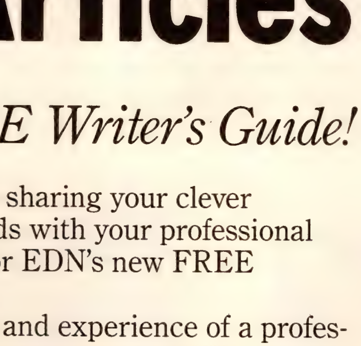

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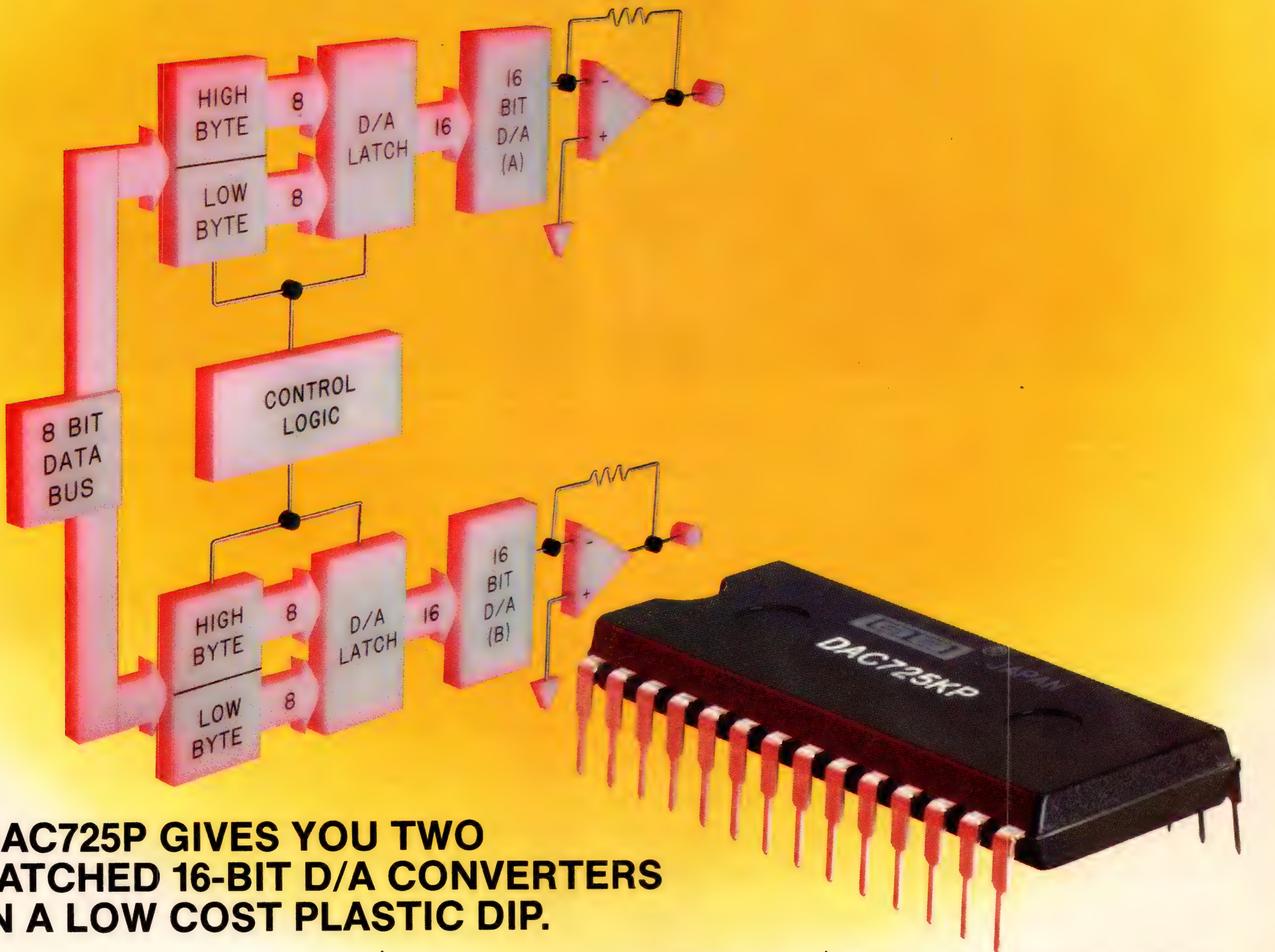
New dual 16-bit DAC saves space, time, and money.



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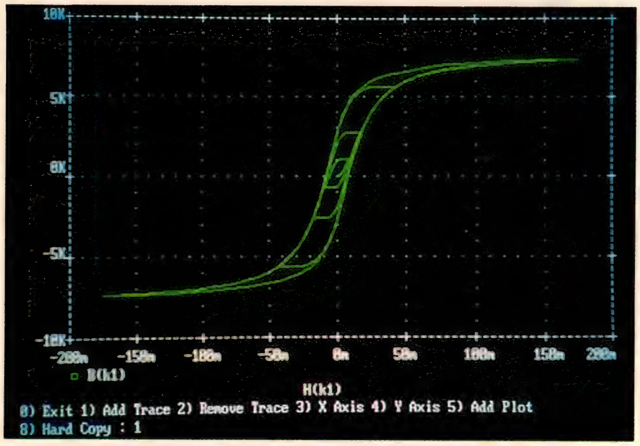
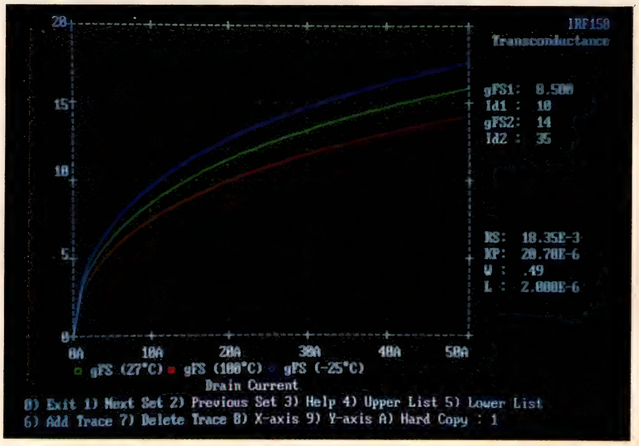
CIRCLE NO 106

PSpice

Simulation With Enhancements for Power Electronics



B-H curve from a core in the PSpice transformer library


20
15
10
5
0
0A
10A
20A
30A
40A
50A
gFS (27°C)
gFS (100°C)
gFS (-25°C)
Drain Current
IRF150
Transconductance
0) Exit 1) Next Set 2) Previous Set 3) Help 4) Upper List 5) Lower List
6) Add Trace 7) Delete Trace 8) X-axis 9) Y-axis A) Hard Copy : 1

gFS1: 8.500
Id1 : 10
gFS2: 14
Id2 : 35

RS: 10.35E-3
KP: 20.70E-6
W : .49
L : 2.000E-6

Characterizing a power MOSFET using Parts

Since its introduction four years ago, MicroSim's PSpice has sold more copies than all other SPICE-type simulators combined. Many of these customers work with power electronics. Why do so many power designers choose PSpice? *Perhaps because every copy of PSpice includes these features:*

- A non-linear magnetics model based on the Jiles-Atherton ferromagnetic equations. It models saturation, hysteresis, eddy current losses, and air gap effects. Instead of approximating the core by using separate equations for different operating regions and then "gluing" the results together, the PSpice model uses one set of equations which describes the core's entire behavior.
- A library of power MOSFET's. The MOSFET equations in PSpice have been enhanced to allow more convenient and accurate modeling of power devices.
- Ideal switches. Logarithmic interpolation for the ON/OFF transition avoids numerical problems.

Or perhaps because of these options available for PSpice:

- Monte Carlo analysis to calculate the effect of parameter tolerances on circuit performance.
- The Probe "software oscilloscope", allowing interactive viewing of simulation results. The left photograph above is a Probe display.
- The Parts parameter extraction program, allowing you to extract a device's model parameters from data sheet information. The right photograph above shows a step in characterizing a power MOSFET.

Or perhaps because PSpice is available on these computers:

- The IBM PC family, including the PS/2 and the Compaq 386.
- The Sun 3 workstation.
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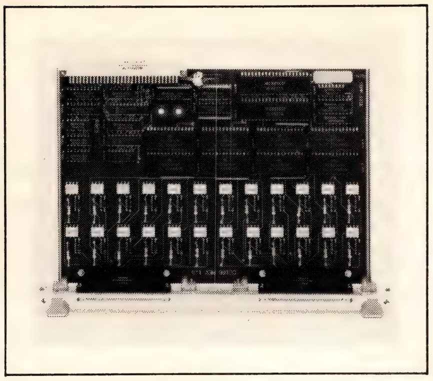

TIMER/COUNTER CARD

- *24 timer/counters with optically isolated clock inputs*
- *Has comprehensive VME Bus interrupt capabilities*

Suitable for use in harsh electrical environments, the CC-106 double-Eurocard VME Bus timer/counter card provides you with 24 independent timer counters, each with an optically isolated clock input. Under software control, you can use the timer/counters to measure frequencies or count events. The maximum input clock rate is 250 kHz. You can generate VME Bus interrupts when individual timer/counters overflow and select a software-programmable interrupt level, interrupt vector, and interrupt mask for each group of three timer/counters. The optically isolated clock inputs are protected against inadvertent overvoltage and reverse-input polarity conditions. The board operates as a VME Bus slave module, occupying 256 memory locations in the 64k-byte VME Bus short-address space. $1425.

Compcontrol bv, Stratumsedijk 31, 5600 AD Eindhoven, The Netherlands. Phone (040) 124955. TLX 51603.

Circle No 362

Compcontrol Inc, 15,466 Los Gatos Blvd, Suite 109-365, Los Gatos, CA 95032. Phone (408) 356-3817. TWX 510-601-2895.

Circle No 363

CPU CARD

- *Runs a 64180 μP and addresses STE Bus memory*
- *Suits software development or target-system use*

Featuring a 6-MHz 64180 CMOS μP, the SC180 STE Bus CPU card suits systems that run banked

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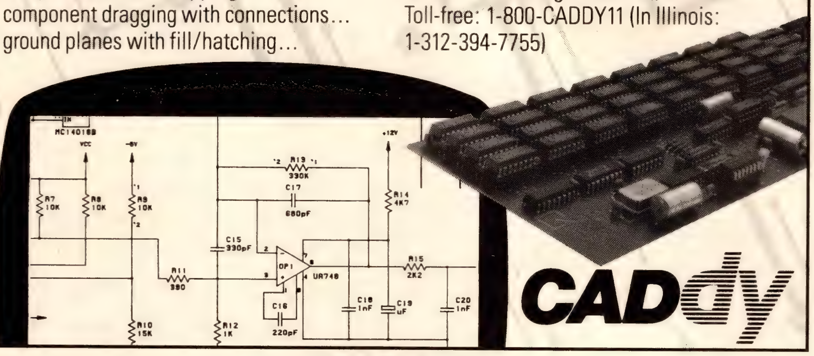

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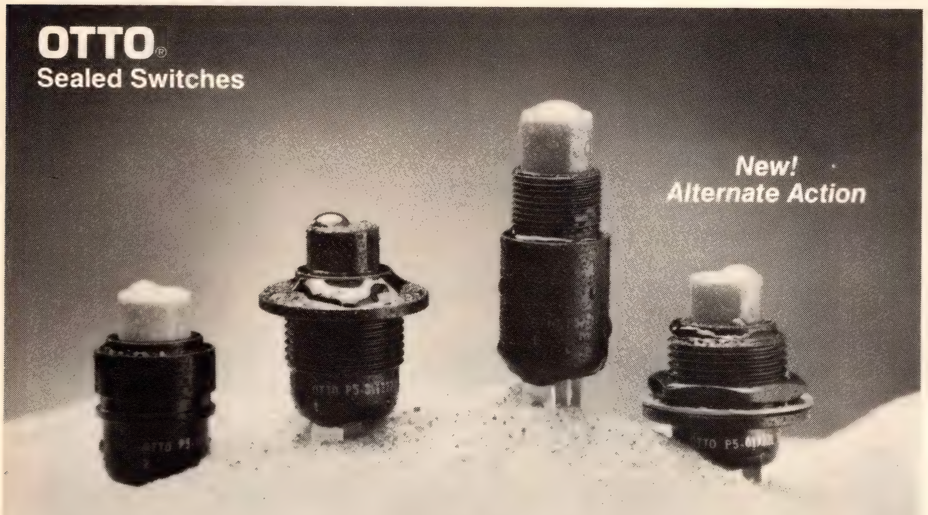

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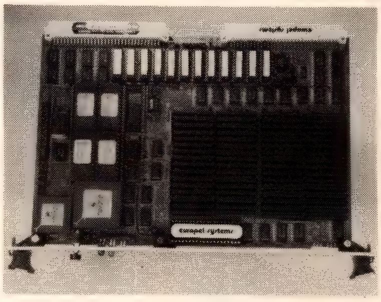
CIRCLE NO 111

CP/M+ applications. The 1M-byte addressing range of this μP allows the CP/M+ operating system to run directly, at optimum speed, without the need for hardware-controlled memory banks. Also provided on the board are four 28-pin memory sockets and a prioritized interrupt handler. You can use the board for software development or as a target system processor. Compiled Basic is available for use with the board. £245.

Arcom Control Systems Ltd, Unit 8, Clifton Rd, Cambridge CB1 4WH, UK. Phone (0223) 411200. TLX 94016424.

Circle No 364



GRAPHICS CARD

- *Achieves screen resolutions as high as 2048×2048 pixels*
- *Can control as many as eight independent screens*

The Opal-2 graphics card for VME Bus systems can output video information at a pixel rate as high as 300 MHz, allowing you to produce interlaced or noninterlaced displays with resolutions as high as 2048×2048 pixels. Alternately, you can use the board's speed to simultaneously control as many as eight independent screens. On color or monochrome screens, you can control the number of bits/pixel at 32 bits/pixel max. When you're using the card to control multiple screens, you can operate different screens at different pixel depths; each screen has its own hardware cursor. The board is controlled by a 16-, 20-, or 25-MHz 68020 μP and a 68881 math coproc-

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CIRCLE NO 112

essor. Hardware accelerators provide block- and area-fill operations, and the board supports hardware windowing, panning, and zooming of the video image. You can directly access the dynamic RAM from the VME Bus. The board also has 64k bytes of CMOS static RAM. The board's master/slave VME Bus interface includes a bus arbiter, interrupter, interrupt handler, and system controller functions. An 8-bit-pixel card with a 40-MHz pixel rate, £4750.

Europel Systems, 5 Vo-Tec Centre, Hambridge Lane, Newbury, Berkshire RG14 5TN, UK. Phone (0635) 31074. TLX 848507.

Circle No 365

GRAPHICS ADAPTER

- *Features VGA compatibility and 256 colors*
- *Provides 800×600-pixel resolution*

The SuperVGA HiRes VGA-compatible graphics-adapter board for the IBM PS/2 computer can simultaneously display 256 colors at 800×600-pixel resolution. You can obtain it with an optional 16-color 1024×768-pixel resolution mode. The board contains 512k bytes of video memory and can support an IBM 8514 monitor. It is compatible with the IBM BIOS VGA and automatic CGA or compatibles. It comes with connectors for analog and TTL/multifrequency monitoring. You can employ one of 10 text modes for spreadsheet and desktop-publishing applications. The unit is also compatible with the Hercules and IBM VGA, EGA, MCGA, CGA, and MDA standards. $695.

Genoa Systems Corp, 73 E Trimble Rd, San Jose, CA 95131. Phone (408) 432-9090. TLX 172319.

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☐ High speed: 16/32-bit temporary register/shifter, 16-bit loop counter, program counter and prefetch pointer, plus dual 16-bit data bus for simultaneous fetching of two operands.

☐ Enhanced interrupt handling: 8 programmable priority levels, hardware context switching for 8 register banks, 8-channel macro service controller.

☐ 256-byte RAM, 16K-byte ROM on-chip; ROM-less version available.

☐ Two stand-by modes: halt and stop.

☐ Package: 84-pin PLCC.

For further information, please contact:
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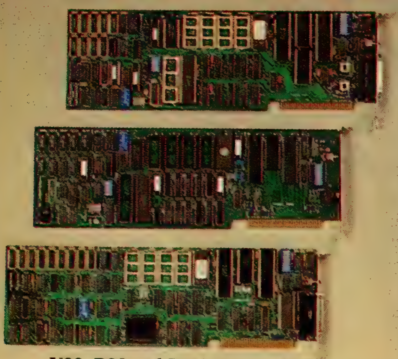
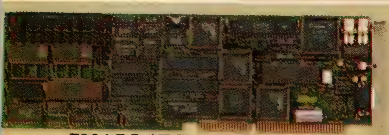
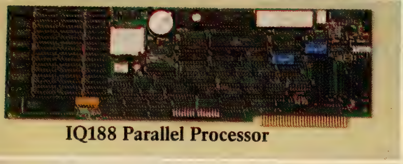
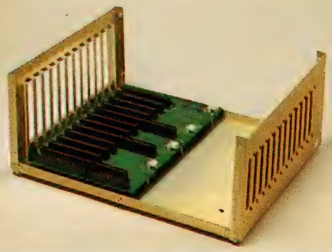

Y88, B88 and R188 PC Bus CPUs


F286 PC-AT Bus 8/10 MHz CPU


IQ188 Parallel Processor

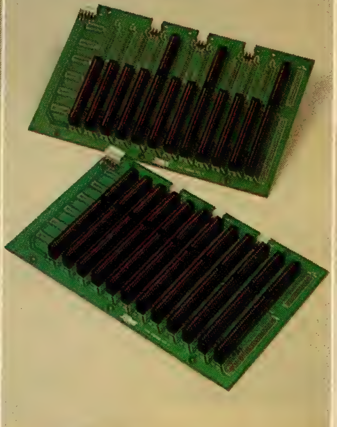
12-Slot PC-AT Bus Card Cage

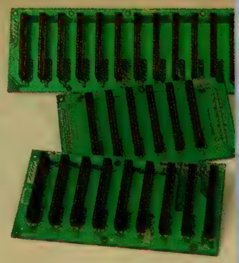


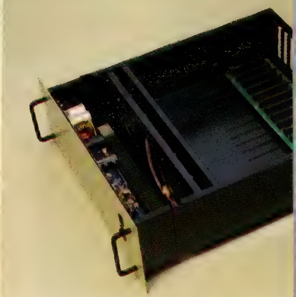
6 and 9-Slot PC Bus Chassis

9-Slot PC Chassis with Two Disk Drive Slots

12-Slot PC-AT Bus Chassis
with Three Disk Drive Slots


PC-AT Bus Backplanes


PC Bus Backplanes


15-Slot PC Bus Chassis

6-Slot PC Bus Chassis
with Two 3½" Disk Drive

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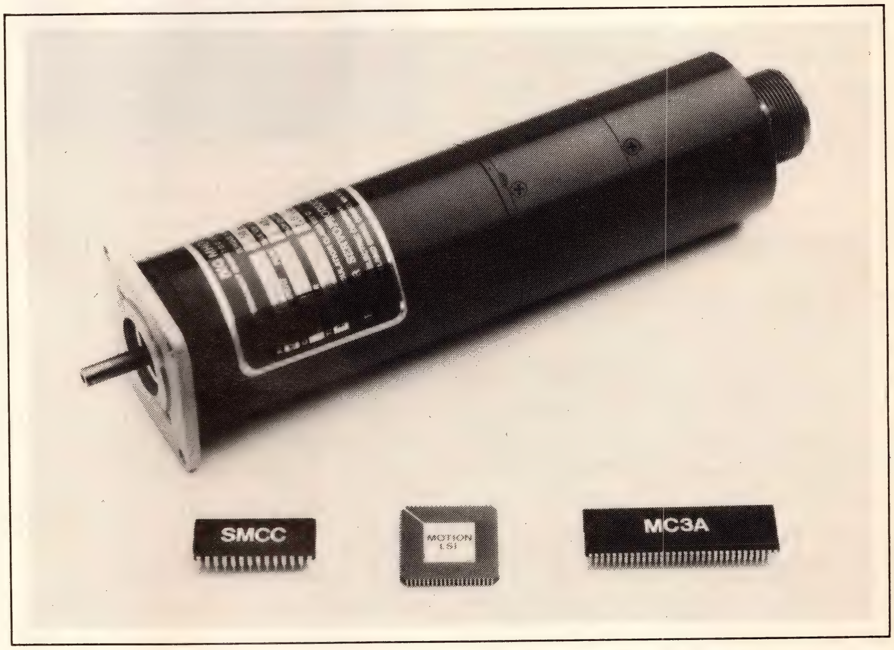
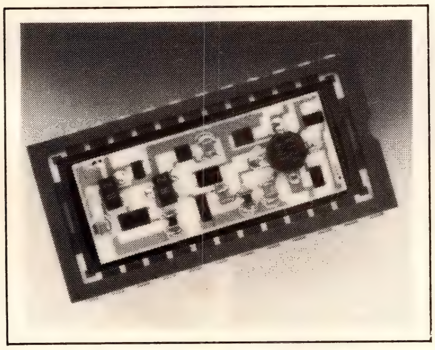
- *Custom 3-chip set*
- *For brushless dc, ac-induction, and stepper motors*



Three custom ICs are available for designing proprietary motion-control systems. The MC3A is a 16-bit internal, 8-bit external, data-bus µP. It has 8k bytes of mask-programmed ROM that holds the servo algorithms and an abbreviated command set for minimum-performance systems. Working with the MC3A is the Motion-LSI chip, which has four channels of A/B quadrature encoder decoding. Internal registers permit software selection of various encoder operating modes. Six digital outputs from the Motion-LSI chip provide PWM signals for the control of 2-, 3-, or 4-phase brushless dc, ac-induction, or stepper motors. The SMCC chip is a 27256 EPROM with a 12k-byte program that extends the command set beyond that contained in the MC3A µP. The 27256 chip comes with the first trial chip set. Thereafter, you must make your own duplications. MC3A µP and Motion-LSI chip, $210 (100).

Delta Tau Data Systems, 21119 Osborne St, Canoga Park, CA 91304. Phone (818) 998-2095.

Circle No 370



HYBRID RF AMPLIFIER

- *Features a GaAs FET front end*
- *14-dB power gain at 500 MHz*

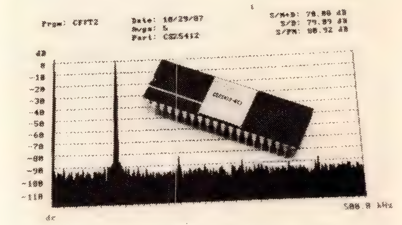
The LH4200 hybrid IC is a 3-stage amplifier that includes a GaAs FET for the front end, and bipolar devices for the second and third stages. This combination results in low noise at high frequencies and high power-output capability. The device's decoupling capacitors eliminate parasitic oscillations without requiring series inductors. The device has a guaranteed power gain of 14 dB at 500 MHz and a noise figure of 3 dB in a 50Ω system. By applying −2V to the input of the FET's second gate, you can obtain as much as 60 dB of gain reduction at 100 MHz, thus making the device useful for a variety of applications that require automatic-gain control. The LH4200 is packaged in a 24-pin ceramic DIP. $54 (100).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 749-7421. TLX 346353.

Circle No 371

1-MHz 12-BIT ADC

- *Low-power monolithic CMOS construction*
- *Guaranteed linearity and harmonic distortion*



According to the vendor, the CSZ5412 is the first monolithic 12-bit ADC to offer 1-MHz throughput. The device's 2-step conversion technique uses complex subcircuit blocks to achieve high resolution and accuracy. Its self-calibration circuitry constantly adjusts linearity to keep the final specification within ±½ LSB. The dynamic range is 72 dB, and the total harmonic distortion is 0.02% max. Its typical power consumption is 700 mW. The device includes a T/H amplifier, a µP interface, 3-state output buffers, and an overrange output, which you can use to signal completion of the self-calibration cycle. You can use the ADC in oscilloscopes, radar, and thermal-imaging systems. It comes in a 40-pin ceramic DIP. From $115 to $187 (100).

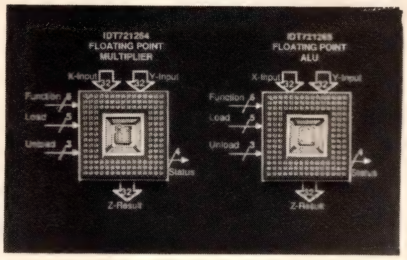
Crystal Semiconductor Corp, Box 17847, Austin, TX 78760. Phone (512) 445-7222. TWX 910-874-1352.

Circle No 372

CHIP SET

- *Floating-point multiplier*
- *Floating-point ALU*

The IDT721264, a multiplier, and the IDT721265, an ALU (arithmetic logic unit), comprise a floating-point chip set that performs 32-bit operations at 33.4M flops and 64-bit operations at 25M flops. The units are pin compatible with the Weitek 1264 and 1265, but feature 30-nsec clock speeds. In addition to providing standard ALU functions, the devices include an instruction that supports the Newton-Raphson algorithm, which simplifies floating-point division operations. The devices conform to IEEE STD 754 version 10.0 and provide an input- to output-register delay of 120 nsec. They operate from a single 5V supply and employ a 3-bus architecture that features two 32-bit input ports and one 32-bit output port. In a 144-pin PGA package, $406 each (100).



Integrated Device Technology, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. TWX 910-338-2070.

Circle No 373

EMBEDDED CONTROLLER

- *8-bit controller offers 16-bit performance*
- *Provides a stepping-stone from 8- to 16-bit microcontrollers*

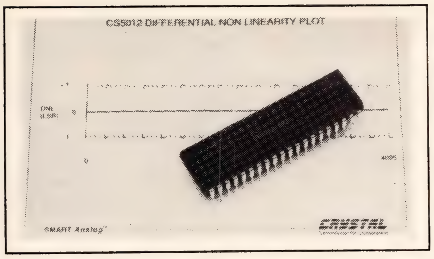
Suitable for real-time 8-bit control applications, the 8098 is an 8-bit external bus version of the 16-bit 8096. Its on-chip features include a 10-bit A/D converter, 32 I/O lines, a 16-bit CPU, 8k bytes of program memory, and 232 bytes of general-purpose registers. The device, which offers the same 16-bit CPU and onboard peripherals as its 8096 counterpart, provides a low-cost alternative for achieving 16-bit performance in real-time-event and motor-control systems. In a 48-pin PLCC, $4.75 (OEM qty).

Intel Corp, Literature Dept W-407, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (800) 548-4725.

Circle No 374

Color by

Watch Apple's new Macintosh II do for color computing what the original Macintosh did for black & white. Our RAMDAC enables Macintosh II to display some of the finest quality graphics available in a personal computer.



12-BIT ADC

- *Features 7-μsec conversion time*
- *Self-calibrates*

The CS5012-7 features 12-bit accuracy to within ±0.5 LSB max, converts in 7 μsec, and has a 100-kHz throughput. The device's on-chip sample-and-hold amplifier eliminates the need for external components to convert ac signals. The converter incorporates 3-state output buffers and a μP interface. An on-chip microcontroller adjusts the device's linearity, resulting in ±0.25 LSB typ nonlinearity, with no missing codes. The converter features 100-psec aperture jitter. You can obtain the device in a plastic or ceramic DIP. $43.70 (100).

Crystal Semiconductor Corp, Box 17847, 2028 E Saint Elmo Rd, Austin, TX 78760. Phone (512) 445-7222. TLX 910-874-1352.

Circle No 375

CROSSBAR SWITCH

- *Transfers data from multiple sources to multiple destinations*
- *Features 64 I/O pins*

The S618840 crossbar switch eases computer interconnections by providing high-speed switching between input and output ports. Functionally compatible with the 74AS8840, the device features 64 I/O pins arranged in 16 switchable nibbles of 4 bits each. The switch will transmit a single input nibble to any combination of 15 output nibbles or, when operating off registered data, to 16 nibbles, including itself. The device's broad routing capabilities facilitate high data rates. It performs port-to-port switching in 25 nsec. The device features dynamic programmability; you may configure the switch to couple a processor to memory, to another processor, or to I/O ports. $59 (100).

Gould Inc, Semiconductor Div, 3800 Homestead Rd, Santa Clara, CA 95051. Phone (408) 246-0330.

Circle No 376

STATIC RAMs

- *Comply with MIL-STD-883C*
- *Have data inputs and outputs that feature TTL compatibility*

The EDI81256C, EDI8464C, and EDI8832C are 256k×1-, 64k×4-, and 32k×8-bit static RAMs, respectively. Available with speeds ranging from 35 to 55 nsec, the units feature battery-powered backup data-retention capability of 2V/50

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Macintosh II. 640x480 resolution, displays 256 colors simultaneously from a 16.8 million color palette.
Bt453. Triple 8-bit 40 MHz RAMDAC with 256 color lookup table.
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CIRCLE NO 115

"We bet our entire company's future on our partnership with Hitachi."

—Jim Balkcom
President and Chief Executive Officer
Humminbird® Depth Sounders
Techsonic Industries, Inc.

"As the second largest manufacturer of depth-sounding equipment, we were determined to become the leader. We knew it would take a breakthrough in meeting the fisherman's needs.

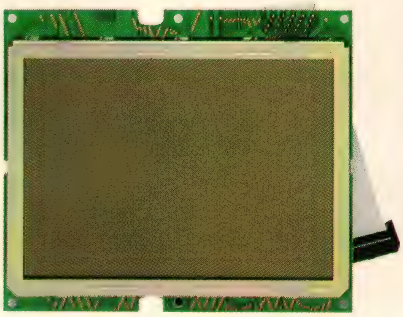
"In strategic partnership with Hitachi, we developed the LCD technology that redefined the depth-sounder market and ultimately quadrupled its size. Our share went from 20 to over 50%. The new technology was a big risk for us. We laid the whole future of our company in Hitachi's hands, and it paid off."

"Whether between two people, or two companies, trust is what makes partnerships work."

"We've shared technologies, design concepts, marketing plans and other critically confidential information across both sides of the table. That's partnership. Trust makes it work . . . and continue to grow."

"Hitachi defines quality the same way we do—meeting customers' needs."

"Hitachi gives Techsonic the technological edge, and more. We've learned it's a waste of time to do incoming testing on Hitachi LCDs. And when we sold over three times our forecast, they were flexible enough to come through for us. Whatever support we need, we get.



And the best part is, we never have to ask for it."

"Hitachi makes it clear that their most important product is our product."

"We needed to team up with an LCD supplier who had the expertise, the capabilities, and the desire to work with us to develop the right solutions. Partnering with Hitachi made Humminbird No. 1, and we're sure it's going to keep us there."

To learn about how partnering with Hitachi can benefit your company, call Tom Klopcic or David Ross at (312) 843-1144. Or write to Hitachi America, Ltd., Electron Tube Division, 300 N. Martingale Road, Suite 600, Schaumburg, IL 60173.

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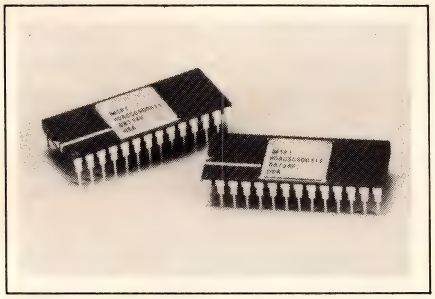
Electron Tube Division

CIRCLE NO 116

μA. The 256k×1- and 64k×4-bit units offer 35-, 45-, and 55-nsec access-time options. The 32k×8-bit unit offers 45- and 55-nsec access times. Each member of the 256k-bit static RAM family operates from a 5V supply. The data inputs and outputs feature TTL compatibility. From $223 to $453 (100).

Electronic Designs Inc, 42 South St, Hopkinton, MA 01748. Phone (617) 435-2341. TLX 948004.

Circle No 377



14-BIT DAC

- *Voltage output of 0 to ±3V*
- *500-nsec settling time*

Fabricated in bipolar-enhanced CMOS (BEMOS), the HDAC50600 DAC maintains 14-bit linearity over its entire operating range. Its output voltage range is 0 to 3V or 0 to ±3V, and on-chip resistors allow you to scale the output voltage to either 5 or 10V full-scale ranges. Both integral and differential nonlinearity are ±½ LSB, and the gain is within ±4 LSBs for the A grade device. The settling time is 500 nsec, and power dissipation is 30 mW. The HDAC50600 is faster than comparable current-output DACs and is μP compatible. Its 100-nsec max write pulse allows it to interface with the fastest μPs without any wait states. It's available in either the industrial or military temperature range in A or B linearity grades. From $21.85 (100).

Honeywell Inc, Signal Processing Technologies, 1150 E Cheyenne Mountain Blvd, Colorado Springs, CO 80906. Phone (303) 577-1000.

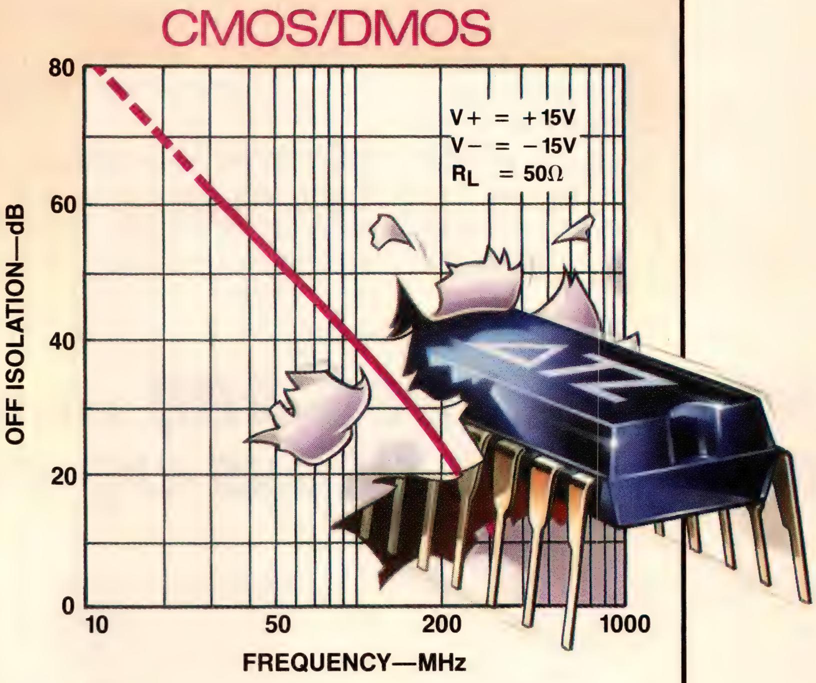
Circle No 378

WIDEBAND OP AMPS

- *Feature 12-MHz compensated bandwidth*
- *Provide 100-MHz uncompensated bandwidth*

The SP-2600 family of op amps offers excellent dc characteristics and bandwidths as high as 100 MHz. The 2600, 2602, and 2605 feature internal compensation and each provide a 12-MHz gain-bandwidth product, a 500-MΩ input impedance, and an open-loop voltage gain of 150,000. The 2620, 2622, and 2625 are uncompensated and each offer a 100-MHz gain-bandwidth product, a 500-MΩ input impedance, and a 1-nA input-bias current. You can use the devices in video amplifiers,

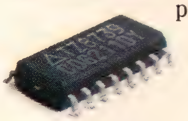
A Breakthrough in Higher Performance.



Topaz combines the best of CMOS and DMOS: high off-isolation at frequencies up to 250 MHz with low insertion loss, achieved only through DMOS, *and* the low-power control circuitry of CMOS.

Our CMOS/DMOS ICs are available in 1x, 2x and 4x SPST analog switches, 2x SPDT with latches, and 4-to-1 multiplexers, all available in standard DIPs and S.O. packages.

Data sheets are available on Topaz CMOS/DMOS products as well as our full line of DMOS FETs, high-frequency analog switches and digitally controlled attenuators. Break through the performance barrier with Topaz products.



TOPAZ
SEMICONDUCTOR

Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799
TEL (408) 942-9100 TWX 910-338-0025 FAX (408) 942-1174

CIRCLE NO 117

high-speed comparators, low-distortion oscillators, buffers for D/A converters, and high-speed S/H amplifiers. All versions come in metal cans, ceramic DIPs, or die form. From $3.01 (100).

Sipex Corp, DataLinear Div, 491 Fairview Way, Milpitas, CA 95035. Phone (408) 945-9080.

Circle No 379

NTSC FIELD BUFFER

- *Provides 263 lines×910 pixels*
- *Features asynchronous read and write capability*

You can use the μPD42270C field buffer IC in digital TV applications and in applications such as teletext system monitoring, broadcast video, and medical imaging. Organized as 263 lines×910 pixels×4-bits/pixel, the device features asynchronous read and write capability, one-field data storage, controllable delay length, and line jump, hold, and reset functions. The IC has a 60-nsec cycle time and a 40-nsec access time. The device allows users to view data in teletext and video-response systems and to implement high-end video telephones. It comes in a 28-pin, 400-mil plastic DIP. The vendor can provide samples now and will begin shipping production quantities in May. $30 (OEM qty).

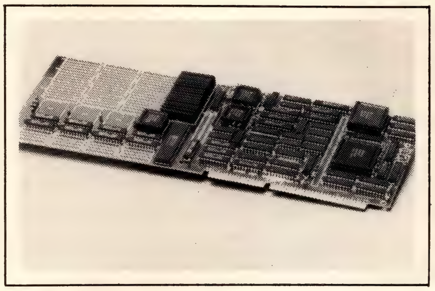
NEC Electronics Inc, Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. TWX 910-379-6985.

Circle No 380

GRAPHICS PROCESSOR

- *20-MHz CMOS chip features a cycle time of 100 nsec*
- *Display-buffer update and video refresh*

The DP8500 raster graphics processor is a high-speed programmable processor for bit-mapped graphics systems. It can operate to 20 MHz and has a cycle time of 100 nsec on back-to-back vector and block operations, thereby boosting the speed of graphics operations. It supports a system architecture that features a constant drawing speed, measured in pixels/sec, independent of the depth (number of bits) of the pixel. The chip's drawing space supports 16384×16384 pixels/bit map, and its text support handles character sizes to 256×256 pixels. The programmable video-refresh function operates at pixel rates as high as 250 MHz and handles display formats to 65536 pixels×4096 scan lines. The DP8500 comes in a 68-pin



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CIRCLE NO 119

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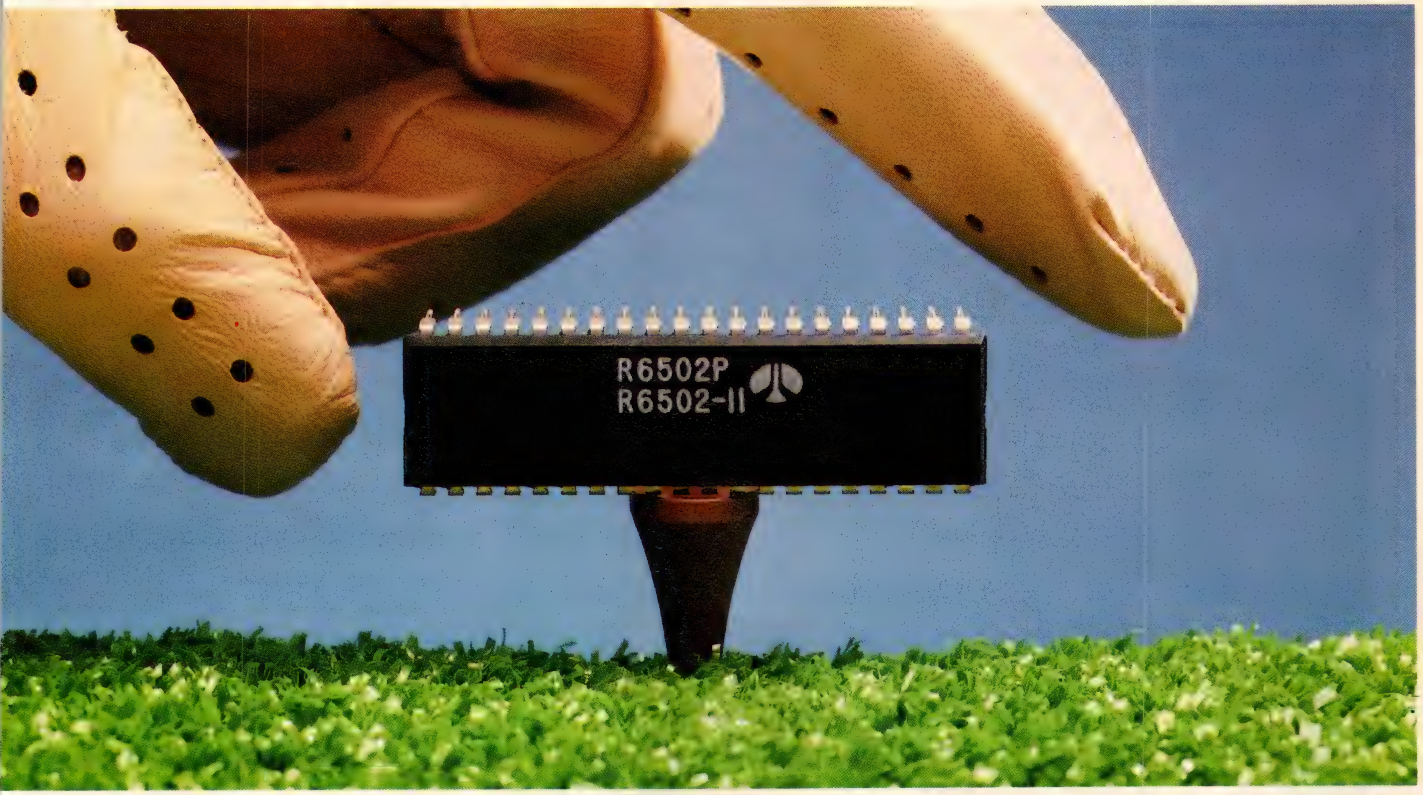

And when it comes to delivering the R6502 family of products from Rockwell, Marshall scores a hole-in-one.

Marshall continues to offer a complete line of high-performance R6502 microcontrollers, microprocessors, and peripheral devices for 8 bit processing applications, including their development systems. Just like we've been doing for over 30 years. We offer broad-line inventory, competitive prices, and delivery schedules that won't leave you in the rough.

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IL Chicago (312) 490-0155*
IN Indianapolis (317) 297-0483*
KS Kansas City (913) 492-3121*
Wichita (316) 264-6333*
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San Antonio (512) 734-5100*
UT Salt Lake City (801) 485-1551*
WA Seattle (206) 747-9100*
WI Wisconsin (414) 797-8400*

CIRCLE NO 120

PLCC. Production quantities will be available in the third quarter of 1988 for $95 (10,000). The DP850EB evaluation board is available now and costs $1495.

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-5404. TWX 910-339-9240.

Circle No 381

SMART POWER SWITCH

- *Switches 500-mA load currents*
- *Detects thermal overloads, and short- and open-circuit loads*

The TDE1799 smart power switch can drive resistive, inductive, or capacitive loads at currents as high as 500 mA. Complementary to the TDE1798, the device is a low-side driver suitable for operation between the negative supply rail and a load connected to the positive supply rail. The IC's output short-circuit protection extends to 32V, and its thermal overload-protection circuitry incorporates a reset control input. Output short circuits, thermal overloads, and open-circuit load conditions activate the switch's alarm. The switch has a differential control input that allows you to use the device with various logic families. Its operating input voltage ranges from 1 to 45V; the input is protected against negative voltages as great as −25V. You can employ switches in parallel to increase the load current. In an 8-pin plastic mini-DIP, $2.90 (1000).

SGS-Thomson Microelectronics, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 382

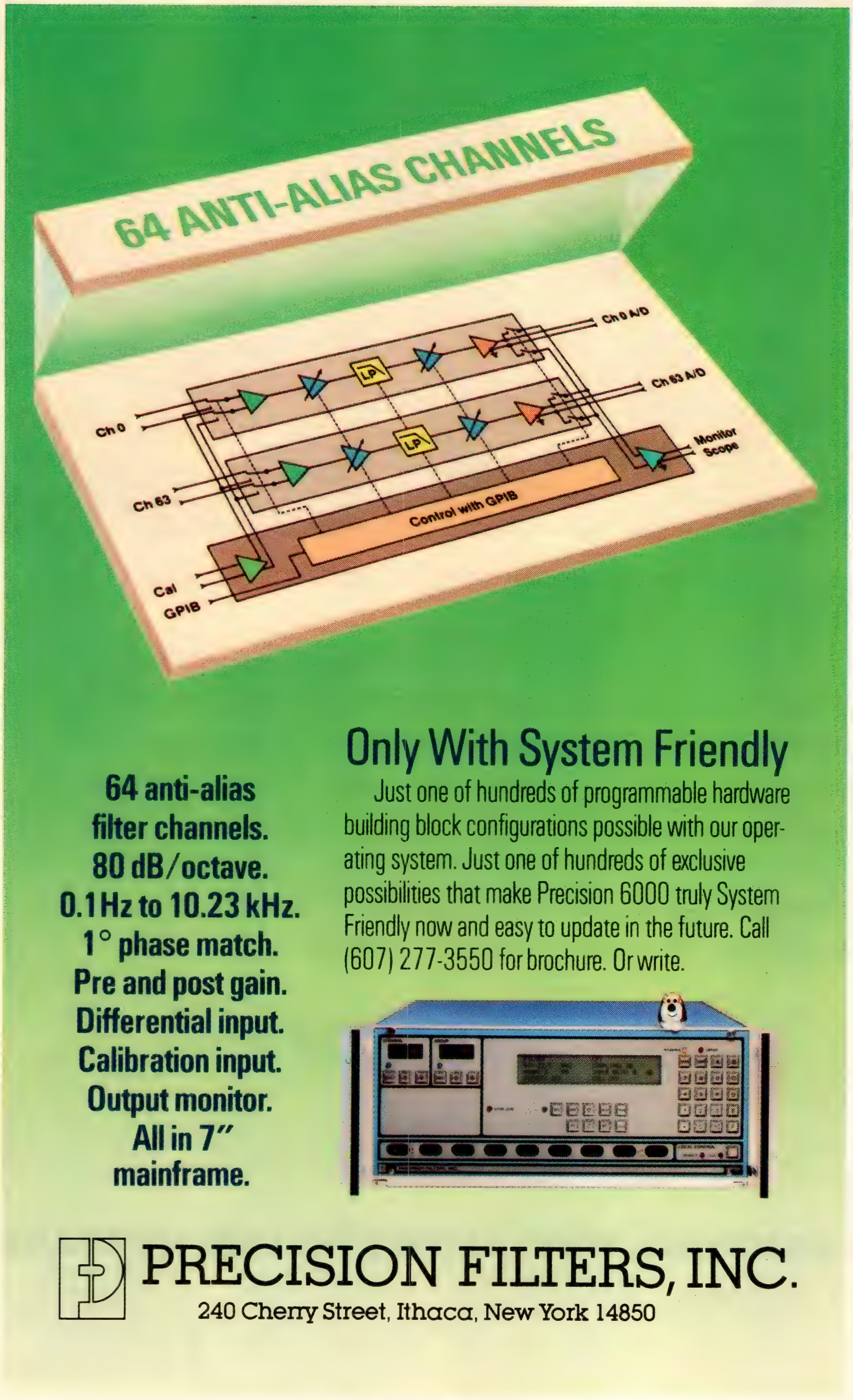
SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 383

DSP CHIP

- *Multiplies two 16+16-bit complex numbers*
- *Can conjugate its inputs to ease complex correlation*

The PDSP16116 complex multiplier can multiply two 16+16-bit complex words to produce a 32+32-bit complex result every 100 nsec. You can use the device in conjunction with two of the vendor's PDSP1601 ALUs and two of its PDSP16316 complex accumulators to produce a block floating-point butterfly processor for evaluating FFTs. By combining the device with a single PDSP16316, you can create a 10-MHz 16×16-bit complex multiplier/accumulator. The device contains four 16×16-array multipliers, two 32-bit adder/subtractors, and control logic that provides fully auto-



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PRECISION FILTERS, INC.
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CIRCLE NO 121

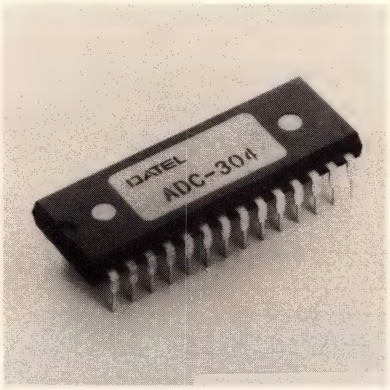
matic block floating-point operation. It also includes trap logic to prevent −1×−1 products from leading to erroneous results. You can cause the IC to conjugate either input and thereby ease the implementation of complex correlators. A single pipeline delay allows you to use the device with recursive algorithms. You can obtain the IC in either a military or industrial temperature range version. For the industrial temperature range, £331.43 (100).

Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wiltshire SN2 2QW, UK. Phone (0793) 36251. TLX 449637.

Circle No 384

Plessey Semiconductors, 9 Parker, Irvine, CA 92718. Phone (714) 472-0303.

Circle No 385



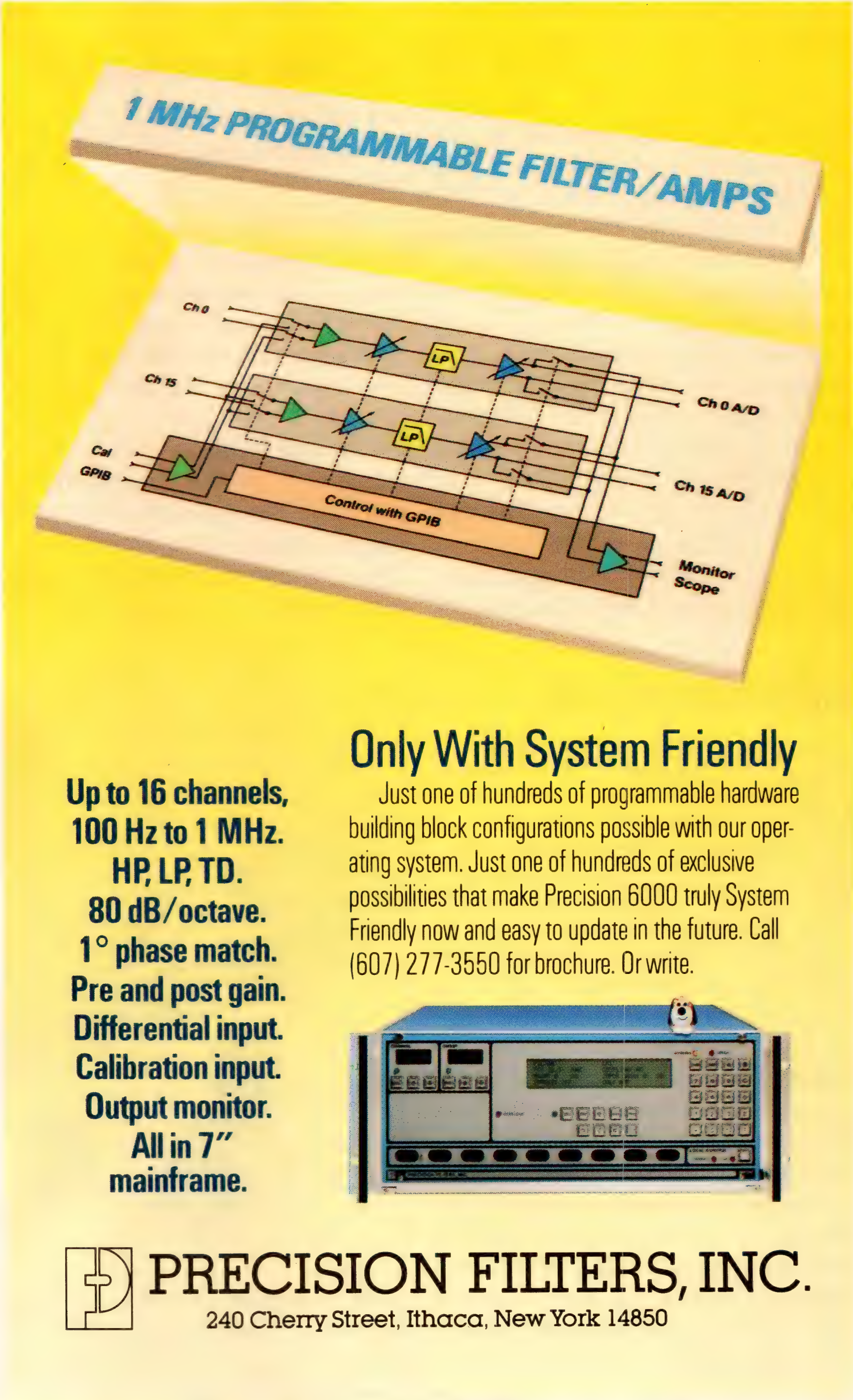
ADC/SAMPLING BOARD

- *½-LSB nonlinearity*
- *20-MHz conversion rate*

The ADC-304 A/D flash converter and the ADC-B304E A/D sampling board are both TTL compatible and provide an 8-MHz analog-input bandwidth. Using a single 5V supply, the ADC-304 provides an input range of 3 to 5V. A 0 to −2V input range is available, using a ±5V supply. The ADC-304 features user-selectable output coding in binary, complementary binary, or complementary two's complement via the LINV and MINV pins. The data-acquisition applications include radar, sonar, and video imaging. Housed in a 28-pin DIP, the device operates over a −20 to +75°C temperature range. The ADC-B304E sampling board is a complete A/D conversion board containing a buffer amplifier, gain adjustment, and filtering and timing circuitry. It's packaged on a standard Eurocard and operates over a 0 to 70°C temperature range. The board has a 20-MHz sampling rate. Applications include high-speed data acquisition, voice signal analysis, video signal processing, and radar imaging. ADC-304 $45; ADC-B304E $350.

GE Datel, 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-9341. TWX 710-346-1953.

Circle No 386



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CIRCLE NO 121

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

PRESSURE SENSOR

- *Features ±0.1% accuracy*
- *In gauge, absolute, and differential pressures*

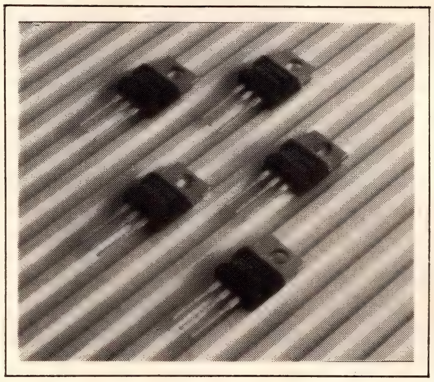
The Model 1220 piezoresistive sensor measures full-scale pressures of 0 to 2 through 0 to 100 psi with accuracies of ±0.1%. Versions are available for gauge, absolute, and differential pressure measurements. The gauge-type unit is compatible with both liquid and gas media. Operating with a 1.235V standard reference, the sensor has a ±1% interchangeability spec. Custom versions that accommodate reference voltages of 0.35 to 7V are available. The standard sensor operates over a −40 to +125°C range and includes temperature compensation of 0.02%/°C for both span and zero adjustment from 0 to 50°C. The unit is housed in an 8-pin DIP and features 0.125-in.-diameter pressure ports. Various lead and pressure-port options let you customize the sensor for specific applications. From $10 (OEM qty). Delivery, stock to six weeks ARO.

IC Sensors Inc, 1701 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1800.

Circle No 390

VOLTAGE REGULATORS

- *Feature a drop-out voltage of 450 mV for an output current of 1A*
- *For output voltages of 5, 8.5, 10, and 12V*



The low drop-out voltage of L4940 Series 1.5A voltage regulators suits them for use as postregulators or as voltage regulators for battery-powered equipment. At an output current of 1A, they have a typical drop-out voltage of 450 mV. They feature a quiescent ground-pin current of 35 mA typ! Their regulation performance is guaranteed over the entire input voltage range and for output capacitances as low as 10 μF. The series comprises four regulators, with output voltages of 5, 8.5, 10, and 12V, respectively. The regulators come in TO-220 plastic packages. $1.20 (1000).

SGS-Thomson Microelectronics, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

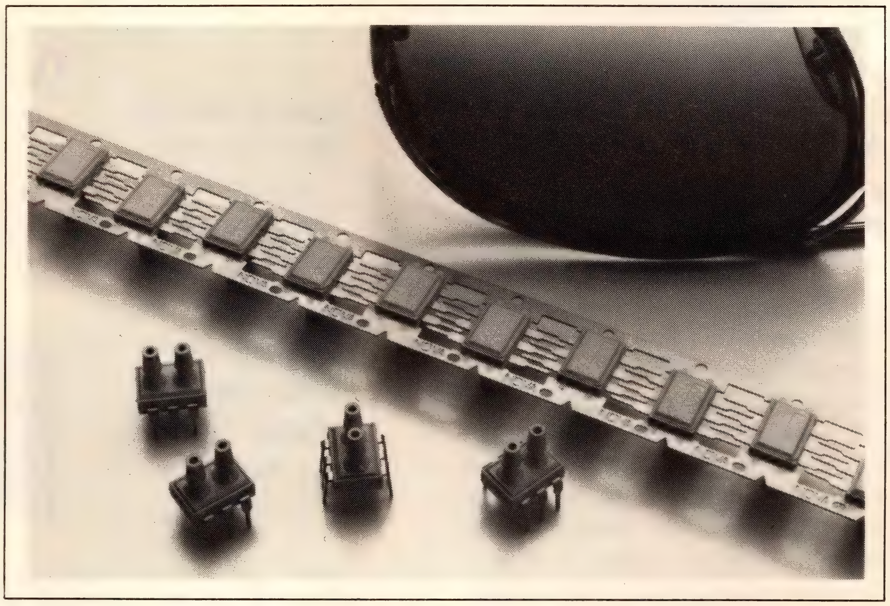
Circle No 391

SGS-Thomson Microelectronics, 1000 E Bell Ave, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 392

PRESSURE SENSOR

- *Available in four differential pressure ranges*
- *Mounts on pc boards*



Packaged in plastic lead frames, the NPS Series pressure sensor features two pressure ports that are compatible with 1/16-in. plastic tubing. The sensor mounts on a pc board and accommodates either top- or bottom-entry tube configurations. The sensor employs ion-implanted piezoresistors in a standard Wheatstone-bridge configuration. They are available in four differential pressure ranges covering 0 to 5 through 0 to 100 psi. The output signal is 100 mV at 1.5 mA. Combined pressure nonlinearity, hysteresis, and repeatability is 0.1% of full-scale output. The sensor package provides three times overpressure protection at 100 psi without degrading performance. $10 (100). Evaluation-quantity delivery, two to eight weeks ARO.

NovaSensor, 1055 Mission Ct, Fremont, CA 94539. Phone (415) 490-9100. TLX 990010.

Circle No 393

Switching Times

TELEDYNE RELAYS
Innovations In Switching Technology

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MAGLATCH NOW CMOS COMPATIBLE

Maglatch Low Power and Indestructible Memory Ideal For Aircraft and Space

Teledyne Relays has introduced a new CMOS compatible Centigrid® version of its popular TO-5 Maglatch relay. This 122C relay is set with a short pulse of coil voltage and retains its state until it is reset, even if the system power fails or is shut off. Since no holding power is required, the 122C is also ideal where power is at a premium. A power FET driver in each input enables direct relay interfacing with CMOS and most other logic families. In addition, its small footprint is well-suited to the newest high-density printed circuit boards. For RF switching applications, the inherently low intercontact capacitance of the 122C provides high isolation and low insertion loss up through 1GHz. The 122C is built to meet the requirements of established reliability mil specs MIL-R-28776 and can be screened to P level. Teledyne's non-latching CMOS compatible relays introduced earlier are already QPL approved to MIL-R-28776/7 and /8.

2 Amp TO-5 Relay In Squib Firing Application

The new 2 amp version of Teledyne's proven TO-5 relay is finding new uses, including squib firing applications. The 212 Series TO-5 relay combines the small package—only .390 inches high—and the time-tested Teledyne reliability which are required for squib firing and other military applications. The 212 Series TO-5 relay is also ideal for controlling small motor loads, lamp loads, and capacitive loads, where current surge at turn-on and turn-off run as high as 2 amps. An innovative proprietary contact system, called TELESIUM,™ makes the higher power level possible and also gives the 212 Series a resistive load rating up to 2 amperes for 100,000 operations.

Teledyne Solid State Introduces New ATE Relay

New C66 Solid State Relay was developed for use in automotive diagnostic test equipment, but other applications are emerging. When this device is turned off it has an extraordinarily low leakage (50 nanoamps). The hermetically sealed units are only 0.458″ square and 0.190″ high and have current ratings of from ±0.3 amp at ±380 volts to ±1 amp at ±200 volts. They are available from Teledyne Solid State now.

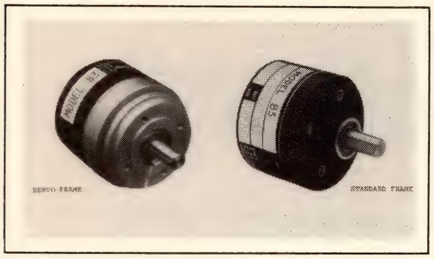
For More Information

Teledyne Relays, 12525 Daphne Ave., Hawthorne, California 90250 • (213) 777-0077/**European Headquarters: W. Germany:** Abraham Lincoln Strasse 38-42, 6200 Wiesbaden/ **Belgium:** 181 Chaussee de la Hulpe, 1170 Brussels/ **U.K.:** The Harlequin Centre, Southall Lane, Southall, Middlesex, UB2 5NH/ **Japan:** Taikoh No. 3 Building, 2-10-7 Shibuya, Shibuya-Ku, Tokyo 150/ **France:** 85-87 Rue Anatole-France, 92300 Levallois-Perret.

Teledyne Supplies Hi-Rel Space Programs

Teledyne's dedication to reliability has made its TO-5 relay the choice of virtually every space program in the Free World. Expanded NASA and Military use of Teledyne's TO-5 for space applications reliability is vertical integration. All piece parts are produced, and critical manufacturing processes are controlled in-house. Teledyne's dedicated "Blue Traveler" hi-rel production line provides utilizing 2-micron small particle cleaning prior to hermetic sealing. All hi-rel TO-5s must pass rigorous functional and environmental screening tests to assure "spaceworthiness." An asynchronous miss test

CIRCLE NO 123



ENCODER

- *Provides quadrature outputs with marker pulse*
- *Housing meets 94V-0 UL requirements*

The Model 83 incremental shaft encoder features quadrature outputs with an index marker pulse and offers resolutions ranging to 1400 pulses per revolution. The outputs are TTL and CMOS compatible. For a light source, the unit uses a single LED that has a useful-life spec of 100,000 hours min. The housing meets 94V-0 UL flammability requirements, and the shielded termination cable is UL/CSA approved. The encoder is available in either round or servo-mount type housings. Its operating range specs at 0 to 70°C. $79 (100). Delivery, six weeks ARO.

Litton Encoder, 20745 Nordhoff St, Chatsworth, CA 91311. Phone (818) 341-6161.

Circle No 394

POWER MODULES

- *Meet UL544 requirements for medical equipment*
- *Feature split-bobbin transformers for high resolution*

The MED300 and MED500 series of ac/dc encapsulated power modules meet the UL544 requirements for medical equipment. They incorporate split-bobbin-wound transformers that provide 2500V ac isolation and leakage current of 10 µA. All the units feature overload, overtemperature, and short-circuit protection. You can obtain single-, dual-, and triple-output versions in various combinations—5, 12, 15, 24V. The modules' output power ranges from 1 to 15W. The vendor supplies the modules in pc-board and chassis-mountable configurations. Both series are UL recognized and CSA certified. 12V/400 mA model, $72.80 (100).

Computer Products Inc, 2900 Gateway Dr, Pompano Beach, FL 33069. Phone (305) 974-5500. TWX 510-956-3098.

Circle No 395

You Don't Need a Thousand Words When You Have a Picture Like This!

Unretouched photograph
*3.5 NS max. rise & fall time measured at CRT cathode.

The image quality demonstrated here is required by your customers . . . and will be appreciated! They expect THE BEST from original equipment manufacturers. You can provide it! While other video monitor venders claim, "about 100 + MHZ" video bandwidth, **Video Monitors, Inc.** *provides it! While other vendors claim, "full gray-scale color capability,"* **VMI** *delivers it!*

And if your customers or you need semi-custom or custom designs, **VMI** *can provide this service. These are just a few of the reasons why* **Video Monitors, Inc.** *should be your supplier of very high resolution monitors.*

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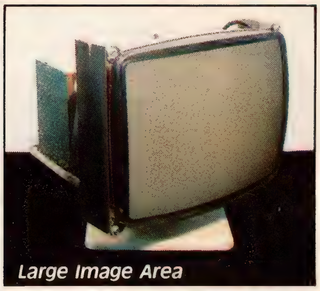
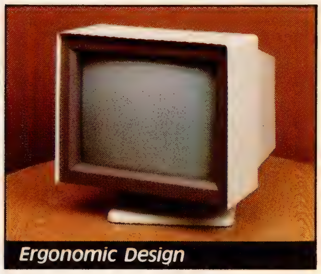

Large Image Area


Ergonomic Design

State-of-the-Art Technology

CIRCLE NO 124

KEYPAD

- *Features a total environmental seal*
- *EMI shielding is standard*

When mounted to a panel, Series 84 4×4-position keypads are completely sealed to the environment. A military-grade silicone rubber boot seals the contact system and also serves as the mounting seal. The snap-dome contact system provides tactile feedback for the operator. The contact side of the dome is gold plated to ensure low contact resistance for 3×10^6 operations per position. EMI shielding is a standard keypad feature. The buttons are located on 0.75-in. centers and are removable and interchangeable. The standard button color is white and legends employ a black epoxy ink that bonds with the button's plastic surface. Special legends and button colors are available. $25.85 (100). Delivery, six to eight weeks ARO for production qty.

Grayhill Inc, Box 10373, LaGrange, IL 60525. Phone (312) 354-1040.

Circle No 396

VF DISPLAY

- *Requires only 5V for operation*
- *Comes in a compact package*

At 7.85×2.5×1.1 in., the 2-line×40-character 3601-86-080 vacuum fluorescent display is smaller than many 1-line×40-character displays. Its 5×7 dot-matrix characters have a height of 0.18 in. Its onboard µP controller handles all scan, refresh, and data I/O tasks, making it easy for you to interface the display to an 8-bit ASCII parallel data bus. The display module operates on a 5V supply. It displays 96 upper- and lower-case letters, as well as numbers and symbols. Its standard display color is blue-green but the vendor offers a wide variety of color filters. $111 (100). Delivery, four to six weeks ARO.

IEE Inc, Industrial Products Div, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

Circle No 397

DISPLAY

- *Viewable in ambient light*
- *Features a 20:1 contrast ratio*

The EL8358HR is a 640×400-pixel IBM EGA-compatible electroluminescent display. Well-suited to MS-DOS applications, the display is viewable in all ambient light and provides a 5×8-in., high-resolution,

SUPER
HIGH RESOLUTION
DOT-X™
DISPLAYS

Dotronix Engineers work closely with you to design products that meet your exacting requirements.

Monochrome Displays from 3″ to 25″
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CAD/CAM/CAE and Graphics
Medical Imaging/Diagnostics
Bank/Brokerage Terminals
Airline Flight Information
Government/Military
Industrial Process Control
Test and Measurement Instruments
Closed Circuit TV Security Systems

Includes the full product line of Video Monitors, Incorporated, a subsidiary of Dotronix, Inc.

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(612) 633-1742 TWX: 9105633541
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Facilities in Minnesota, Wisconsin and Taiwan

CIRCLE NO 125

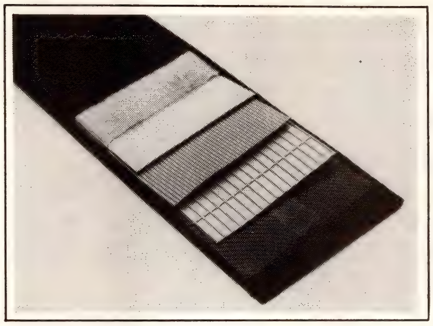
yellow, active-matrix area. The display has a 20:1 contrast ratio. Its viewing angle specs at 160°, and its power consumption equals 5 to 10W. The display's EGA compatibility makes it suitable for industrial markets that use MS-DOS utility or graphics software packages. $675 (OEM qty).

Planar Systems Inc, 1400 NW Compton Dr, Beaverton, OR 97006. Phone (503) 690-1100.

Circle No 398

FLAT CABLE

- *High impedance/low capacitance and full shielding*
- *Complies with FCC regulations for EMI/ESD protection*



In addition to providing high impedance and low capacitance, the 3751 PVC flat cable offers full shielding. It's designed for applications involving certain DEC Q Bus- and Unibus-compatible peripherals. The cable also helps you comply with FCC regulations for EMI/ESD protection; it features a full 360° wrap of extended copper shield. Dielectric PVC material, located above and below the cable inside the shield, maintains precise shield-cable spacing, thus providing the high-impedance and low-capacitance values. The cable is available with 26, 40, and 50 28 AWG conductors on a 0.05-in. center pitch. The impedance measures 90Ω with connectors in ground-signal-ground configuration and 115Ω in the signal-to-ground shield configuration. The capacitance specs at 17.4 pF/ft. $3.20/ft (1000 ft) for 40-conductor cable.

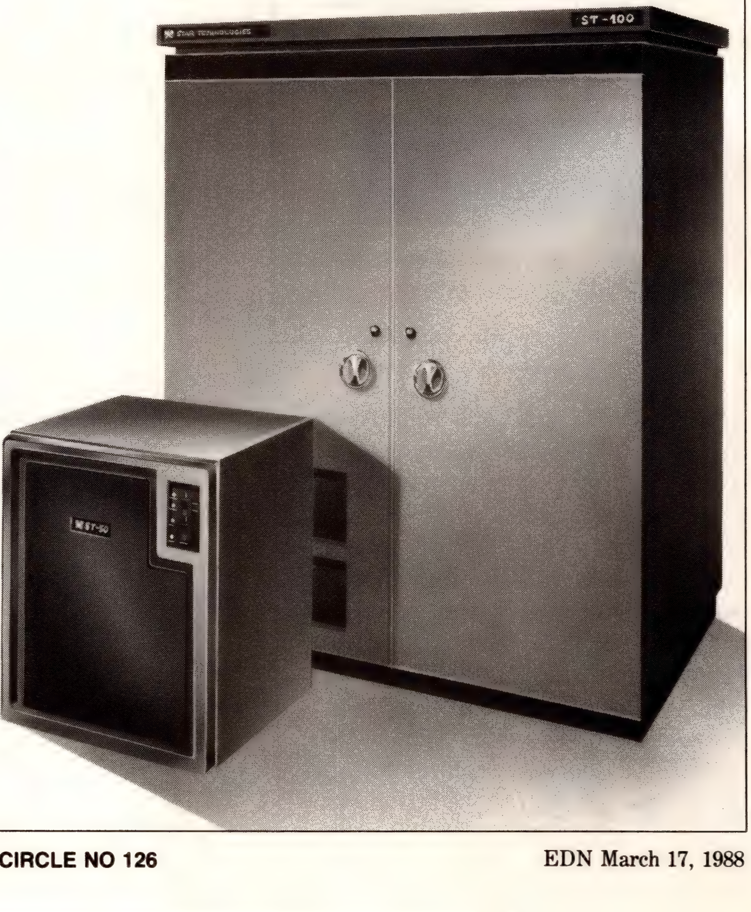
3M, Box 2963, Austin, TX 78769. Phone (512) 834-1800.

Circle No 399

SWITCHES

- *Feature 1 million-actuation lifetime*
- *Meet military requirements*

You can use water-clear Touch-View screens as transparent switches or control elements for direct placement over CRTs, alphanumeric readouts, or backlit displays. The conductive switch elements are made by depositing indium tin oxide onto a stabilized polyester base. You can place the switches in any location along the X-Y axis of the screen at 0.5-in. center-to-center spacings. The vendor can also configure the



The only thing faster costs millions more.

The ST-100 32-bit array processor gives your host the power of a supercomputer. So you can get 100 megaflops of computing capability from your current mainframe or superminicomputer. And get Cray 1 speed for less than $300,000.

Not surprisingly, this kind of price-performance relationship makes the ST-100 an ideal companion for even the fastest host.

Just ask any of the engineers and scientists in industry and government using the ST-100 for high-speed time-critical applications in image processing, signal processing, medical diagnostics, modeling and simulation.

And our other products, including the compact 50 megaflops ST-50, also provide powerful and economical processing alternatives.

If you need the power of a supercomputer but don't have a super budget, call us today at (800) 782-7005. **Or call from your modem 1-800-444-8080 (300-1200 baud, 8 bit, no parity 1 stop bit) and enter the access code STAR 1 when prompted.**

And get super speed and reliability at a super price.

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515 Shaw Road, Sterling, Virginia 22170

CIRCLE NO 126

Thanks Datron Instruments...
...we needed this!

A Multifunction Calibrator for DMM's,
In one feature-packed single unit!

- **DC VOLTAGE (10nV to 1100V) 16ppm**
- **AC VOLTAGE (100nV to 1100V) 220ppm**
- **FREQUENCY (10Hz to 1MHz) 100ppm**
- **RESISTANCE (10 Ω to 100 MΩ) 20ppm**
- **DC CURRENT (0.1nA to 2A) 110ppm**
- **AC CURRENT (0.1nA to 2A) 450ppm**
- **RESOLUTION 6½-7½ Digits**
- **AUTOCAL "Covers-on Calibration"**
- **IEEE-488 COMPATIBLE**

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Model **4700**

Also here!
The 4707 Standard and
versatile 4705 models.

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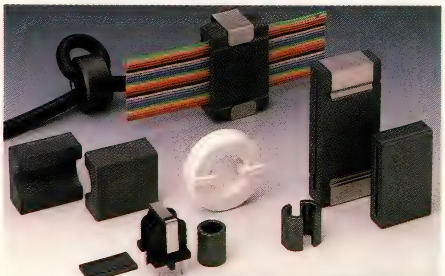
Wavetek Corporation 9191 Towne Centre Drive, Suite 450, San Diego, California 92122 (619) 450-9971
Datron Instruments Ltd. Hurricane Way, Norwich Airport, Norwich NR6 6JB England (0603) 404824 Telex 975173

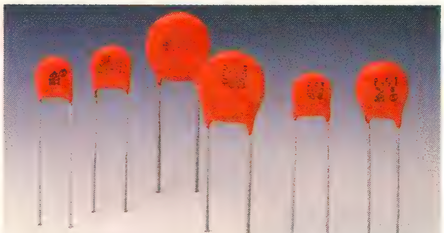
CIRCLE NO 127

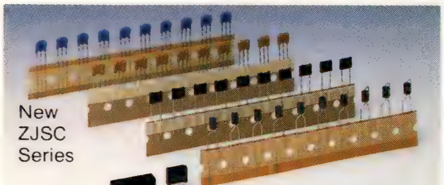
How to Beat EMI/RFI Once and For All!

With high performance TDK EMI/RFI components

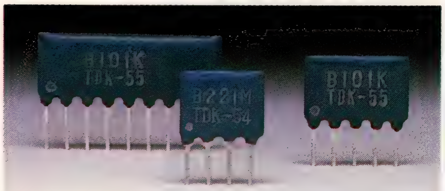
EMI/RFI Suppression Filters


EMI/RFI Suppression Ferrites


UL Recognized (CSA, VDE, SEV, SEMKO, BS) Ceramic Capacitors



Through Hole EMI/RFI Filters



Ceramic Capacitor Networks

With recent advances in digitization and integration, electronic circuits require a higher degree of reliability than ever before. Advanced circuits and devices now have to overcome expanding EMI environments and the tighter international EMI/RFI standards enforced by the FCC, CISPR, and DIN. TDK technology can help.

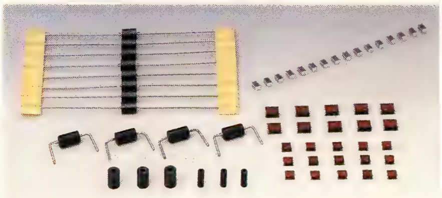
Our expertise in ferrite and other materials technology has produced an outstanding line of noise-beating components, all manufactured according to integrated production processes. We offer every kind of EMI/RFI filter imaginable—from power source filters to through hole filters—to combat noise from the low to high frequency range.

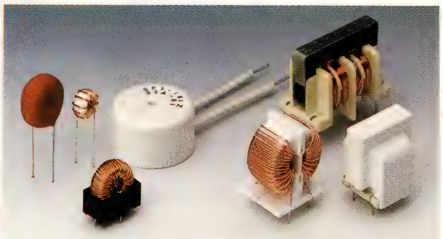
Our products include ferrite cores, amorphous magnetic materials, ceramic capacitors, varistors, radio wave absorbent materials, and electromagnetic shielding materials. All carry the TDK guarantee of reliability, and are suitable for a variety of applications, including advanced computers, automobile electronics, and OA and FA equipment.

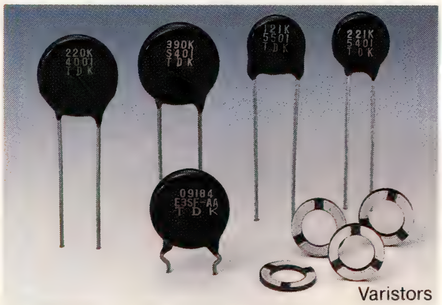
And with TDK, you get more than noise-combatant components. You also get our full support services, whether it's a matter of constructing an electromagnetic wave anechoic chamber, or devising the right measurements.

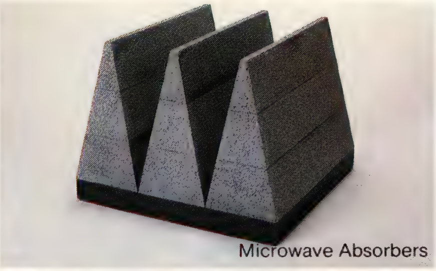
● ● ●

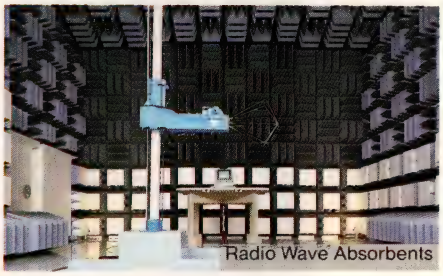
CEL is at your service. CEL, TDK's Component Engineering Laboratory in Torrance, CA, can assist you by custom designing and test manufacturing TDK EMI/RFI Components to meet your specific requirements. Call (213) 530-9397.


Ferrite Beads/Ferrite Chip Beads


Common Mode Choke Coils /Line Choke Coils (SF Type)


Varistors


Microwave Absorbers


Radio Wave Absorbents

TDK Electromagnetic Compatibility Technology—At Your Service!

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TDK CORPORATION OF AMERICA **HEAD OFFICE** 1600 Feehanville Drive, Mount Prospect, IL 60056, U.S.A. Phone: (312) 803-6100 **CHICAGO REGIONAL OFFICE** Phone: (312) 803-6100 **INDIANAPOLIS REGIONAL OFFICE** Phone: (317) 872-0370 **NEW YORK REGIONAL OFFICE** Phone: (516) 625-0100 **LOS ANGELES REGIONAL OFFICE** Phone: (213) 539-6631 **DETROIT DISTRICT OFFICE** Phone: (313) 353-9393 **NEW JERSEY DISTRICT OFFICE** Phone: (201) 736-0023 **HUNTSVILLE DISTRICT OFFICE** Phone: (205) 539-4551 **GREENSBORO DISTRICT OFFICE** Phone: (919) 292-0012 **DALLAS DISTRICT OFFICE** Phone: (214) 506-9800 **SAN FRANCISCO DISTRICT OFFICE** Phone: (408) 437-9585 **TDK CORPORATION**, TOKYO, JAPAN.

CIRCLE NO 128

switches into a linear control element with almost infinite resolution. Applying pressure to different positions of the linear screens produces different resistance values. You can order Touch-View screens with combinations of fixed-position switches and linear-control devices. The vendor has tested the screens over 1 million actuations and can supply screens that meet various military specifications for ground or airborne applications. $55 to $500. Delivery, 10 to 12 weeks ARO.

CAM Graphics Co Inc, 15 Ranick Dr West, Amityville, NY 11701. Phone (516) 842-3400.

Circle No 400

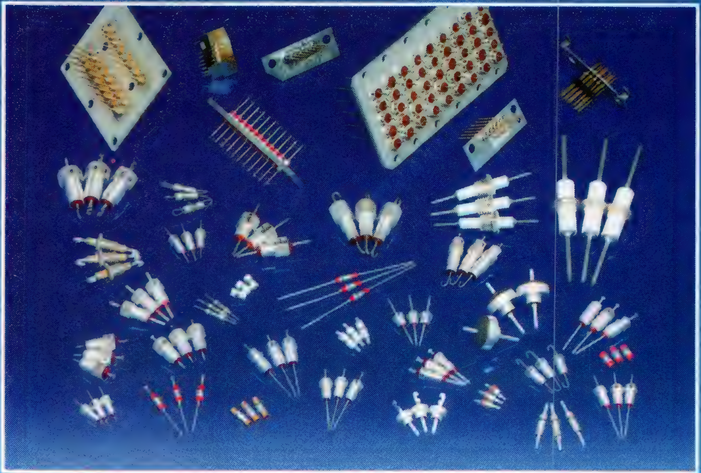
CRYSTAL OSCILLATORS

- *Crystal controlled for high stability*
- *Voltage controlled frequency variation of ±160 ppm*

Suitable for use in the PCM signal-recovery PLLs of telephone exchange or LAN equipment, the 9922 Series voltage-controlled quartz-crystal oscillators feature a pullability of ±160 ppm, and a stability of more than ±20 ppm over their entire operating temperature range. The long-term frequency drift is typically less than one part in 10^5 over a period of 10 years. Standard versions are available with center frequencies of 8.192, 8.448, 11.456, and 14.912 MHz. The company can also provide custom versions for your own frequency requirements. The oscillator's linear-frequency variation over a finite control-voltage range also makes the oscillators suitable for other applications—for example, color-level locking in video/broadcast cameras. Although they operate from a single 5V supply, the oscillators accept bipolar control voltages. Their output is LSTTL-compatible and they consume approximately 30 mW of power. They are housed in 4.9-mm-high, hermetically sealed packages that have leadouts on the same lead spacing as a 14-pin DIP. They operate over a −5 to +60°C temperature range. Approximately Gld 80 in small quantities.

Philips, Components Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757189. TLX 51573.

Circle No 401



TUSONIX

If you're looking for a reliable source for EMI Filters and Custom Filter Assemblies . . .

Tusonix, as a QPL source, is proud of its JIT performance

Miniature EMI/RFI ceramic filters and filter capacitors attenuate most frequency ranges in a wide variety of QPL approved styles. Most are available from stock in production quantities, ready for immediate shipment.

When it comes to custom packaging EMI/RFI feed-thru filters and/or filter capacitors, Tusonix offers a complete in-house custom assembly capability. Every assembly is 100% tested in Tusonix' quality assurance laboratories. The result is a reliable, economic assembly that satisfies your unique needs.

So let Tusonix supply your filter requirements in discrete filters and assemblies. Write for literature TODAY . . . or please call us at:
Phone: 602-744-0400

TUSONIX

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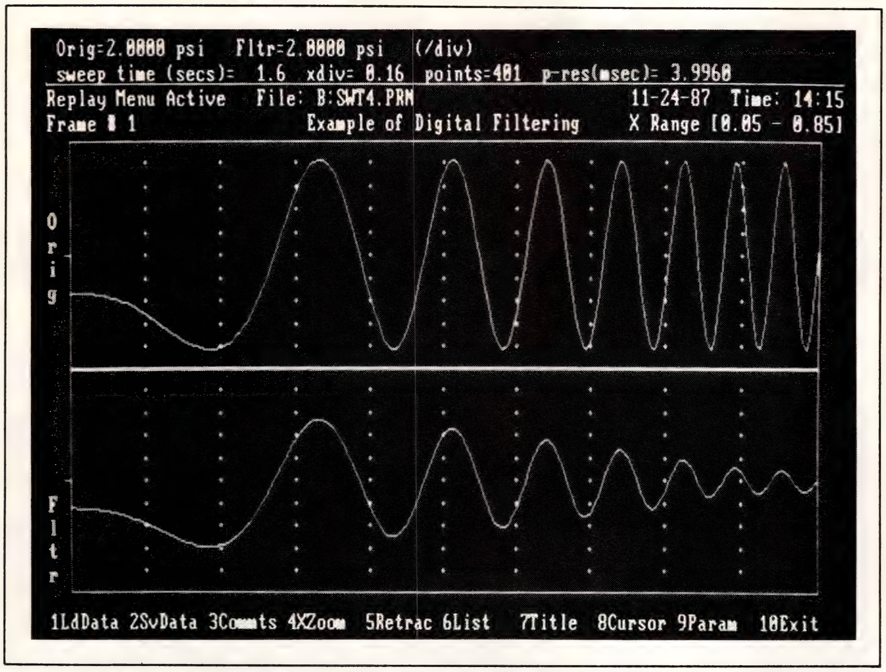
Phone: 602-744-0400 Telex: (RCA) 299-640
FAX: 602-744-6155

CIRCLE NO 129

CAE & SOFTWARE DEVELOPMENT TOOLS



```
Orig=2.0000 psi   Fltr=2.0000 psi   (/div)
sweep time (secs)=  1.6  xdiv= 0.16  points=401  p-res(msec)= 3.9960
Replay Menu Active   File: B:SWT4.PRN                 11-24-87  Time: 14:15
Frame # 1                   Example of Digital Filtering    X Range [0.05 - 0.85]
```

Orig
Fltr
1LdData 2SvData 3Commts 4XZoom 5Retrac 6List 7Title 8Cursor 9Param 10Exit

DIGITAL FILTERING

- *Provides digital filtering on an IBM PC or compatibles*
- *Works with acquisition and analysis software*

Snap-Filter provides four types of filter: lowpass, highpass, bandpass, and band-reject. You can specify all four types as either FIR (finite impulse response) filters, which preserve the time relationship of different signal components; or as IIR (infinite impulse response) filters, which emulate analog filters such as Butterworth and Chebyshev. Simple, 1-letter commands specify the type of filter you want, and you add parameters to specify FIR or IIR and the cutoff frequency (or frequencies). The package works in conjunction with the vendor's Snapshot Storage Scope data-acquisition software and Snap-Calc monitoring and analysis program. All three programs run on the IBM PC and compatibles and work with a wide variety of D/A and A/D converter boards. Combined software package, $1185; Snap-Filter only, $395.

HEM Data Corp, 17025 Crescent Dr, Southfield, MI 48076. Phone (313) 559-5607.

Circle No 405

CAE FOR GATE ARRAYS

- *Low-cost schematic capture for programmable gate arrays*
- *Component library includes more than 3700 parts*

The LCA-MDS151 is a low-cost schematic-capture package that runs on the IBM PC/AT, PS/2, and compatibles. It features an enhanced version of the SDT-III schematic editor from OrCAD (Hillsboro, OR), and Xact, the vendor's design editor for programmable gate arrays. The library consists of OrCAD's library of 3700 parts in addition to the vendor's own programmable-gate-array macro library of TTL and standard logic-family equivalents. You enter your schematics with the aid of the editor, using the library of gates and macros; a software translator converts the schematics into specifications for working programmable gate arrays. Pop-up menus and English-like commands make the system easier to use. The system provides five levels of zoom and automatic pan, 16 user-configurable colors, and more than 100 keyboard macros. LCA-MDS151, $4950; LCA-MDS152, schematic-capture editor without Xact, $1850.

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 406

DESIGN UTILITIES

- *Include rule-checking and format conversion*
- *Statistics on component usage and copper area*

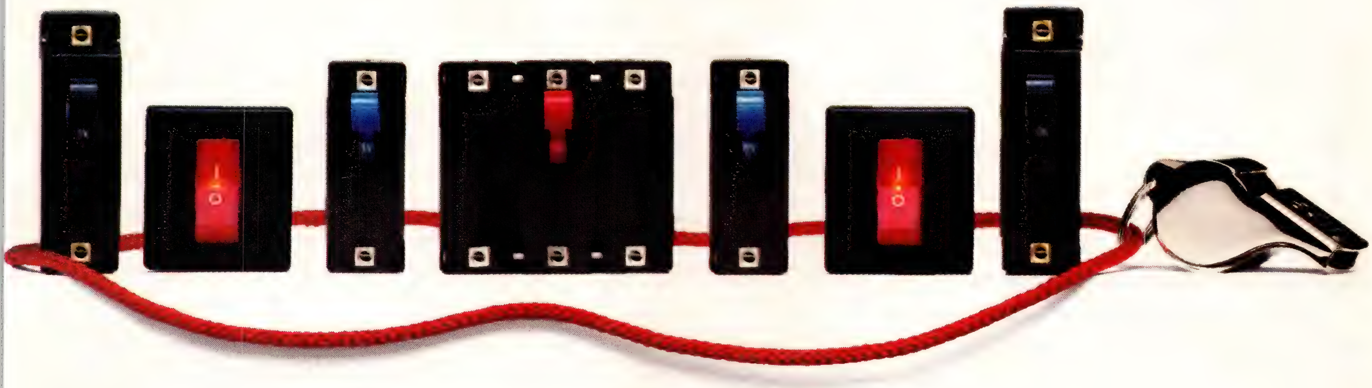
Tango-Tools is a set of utility programs that can help you during the layout, design verification, and artwork generation of pc boards. These tools supplement the facilities of the vendor's schematic capture, pc-board layout, and autorouter programs. A design-rule checker checks your pc-board file for violations of your electrical and clearance rules; a net-list editor helps you create and edit net lists. A Tango-to-DXF converter converts Tango pc-board files to industry-standard DXF (data-exchange format) files. You can then use the DXF files with a wide variety of CAD programs from other vendors. A pc-board file scanner displays the number of power- and ground-plane connections, the number of components, and the area of copper per layer. A menu-driven, layer-swap utility lets you swap layers within a pc board or remove entire layers. The tools run on an IBM PC, PC/XT, PC/AT, PS/2, or compatible computer that has at least 256k bytes of RAM; two disk drives; and monochrome, Hercules, or IBM CGA or EGA,(or com-

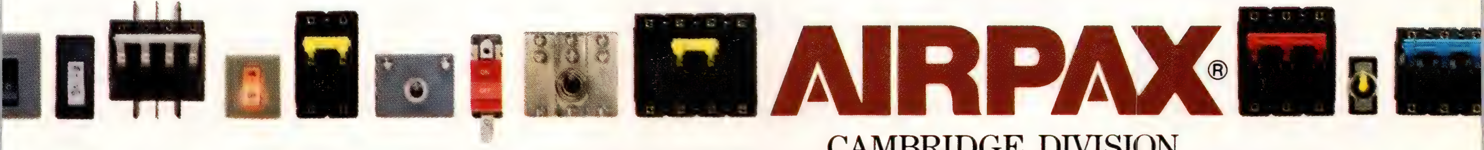
SIMPLY THE BEST DEFENSIVE LINE IN THE GAME.

When it comes to depth, diversity, and a proven winning record, no other line of circuit breakers can compare with ours. The Airpax team is your source for fast response and reliable performance in your choice of more styles, configurations and ratings to meet your specific needs.

We've been tackling the toughest applications for more than thirty years. Chalking up milestone victories such as twenty years of uninterrupted MIL-C-39019 approval in Type AP electromagnetic circuit breakers. Blitzing international markets with the VDE-approved and rail-mount magnetic circuit breakers. Continually striving through innovation to keep you, the Airpax customer, at the forefront of circuit breaker technology.

Draft the best defensive players into your design. Contact Airpax Corporation, Cambridge Division, Woods Road, Cambridge, MD 21613. (301) 228-4600. Telex: 6849138, Fax: (301) 228-8910. A North American Philips Company.





AIRPAX®

CAMBRIDGE DIVISION

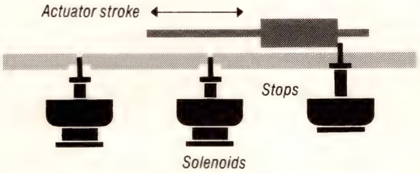
CIRCLE NO 130

Repeat positioning design tips

Ledex solenoids simplify positioning.

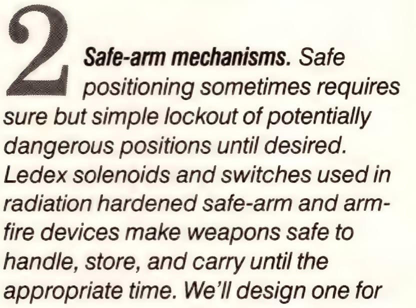
Solenoids can help you position repeatably and accurately. The advantages in automatic control and automation equipment are simplicity, inherent reliability, long life, ease of interfacing, and quick availability from stock. Consider these tips:

1 **Positive stops.** Instead of a position feedback drive, consider a less expensive drive with positive stops activated by solenoids. A control might shut off the drive and switch on the selected stop. A solenoid engaged clutch or brake might be used also.



Push or pull solenoids can be selected for repeatable positioning.

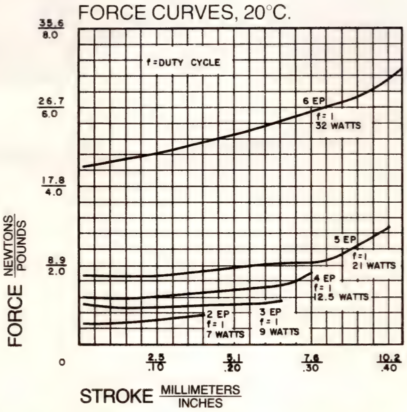
2 **Safe-arm mechanisms.** Safe positioning sometimes requires sure but simple lockout of potentially dangerous positions until desired. Ledex solenoids and switches used in radiation hardened safe-arm and arm-fire devices make weapons safe to handle, store, and carry until the appropriate time. We'll design one for you, or share some hints if you're safe-arming.



Solenoid device in the safe-arm positively positions missile on safe or arm status.

3 **Fail-safe.** A solenoid with a return spring makes an ideal fail-safe device. In the event of power failure, the spring mechanically returns the plunger. Useful in fire doors, for example.

4 **Microprocessor solenoid positioning.** If you're already using a microprocessor, a Soft Shift™ solenoid will give you accurate positioning at low cost. You obtain smooth actuation in a device with 3 to 5 times the starting force of a standard solenoid. Program an input current ramp to vary speed, reduce or eliminate noise. Five stock models, charted below at continuous duty, have return spring.



Want to know more?

Request catalogs.

Ledex Inc.
A Subsidiary of Lucas Industries
P.O. Box 427
Vandalia, Ohio 45377-0427 U.S.A.
Phone: 513-898-3621

LEDEX®

helpful solenoid technology

patible) graphics boards. Until May 1, 1988, $195; thereafter, $295.

Accel Technologies Inc, 7358 Trade St, San Diego, CA 92121. Phone (619) 695-2000.

Circle No 407

PHIGS FOR VAX/VMS

- *Provides device-independent graphics*
- *Allows hidden-surface removal, shading, and depth-cuing*

VAX PHIGS (Programmer's Hierarchical Interactive Graphics System) is a 3-dimensional graphics system that controls the definition, modification, and display of hierarchical graphics data. It provides the interface between application programs and the underlying graphics system in a manner that allows the application program to generate graphical output on a variety of hardware devices without modification of its source code. The graphics system is based on the ANSI draft PHIGS standard, dpANS X3.144-198X, but it contains extensions that permit hidden-surface removal, shading, and depth cuing. It provides Fortran and C bindings, as well as a language-independent binding. $3500.

Digital Equipment Corp, Maynard, MA 01754. Phone local office.

Circle No 408

MONTE CARLO ANALYSIS

- *Provides results in terms of probabilities*
- *Lets you set accuracy limits for each variable*

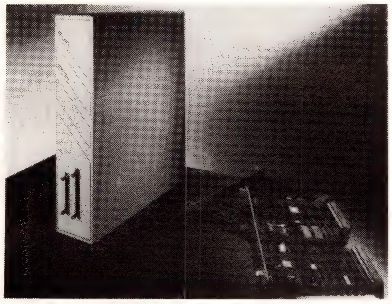
Monte Carlo Plus runs on the IBM PC and compatible computers and performs risk and sensitivity analyses of data contained in a Lotus 1-2-3 spreadsheet. The program prompts you to supply high- and low-accuracy limits for key variables, and then estimates the statistical probability that a particular result computed by the spreadsheet will exceed or fall short of the pre-

CIRCLE NO 131

dicted value. You can also use the program to determine the effect of independent variables on a dependent result; the program identifies the variables that have the least and the greatest effect on the result. The program provides both risk and sensitivity results in the form of tables and graphs. $89.

Suntex National Corp, Box 772868, Houston, TX 77215. Phone (713) 783-9059.

Circle No 410



IN-CIRCUIT EMULATOR

- *Supports a range of popular 8-bit μPs*
- *Includes paged-memory-system emulation*

The Mime-600 in-circuit emulator supports numerous 8-bit μPs, including the 6801, 6803, 6805, 6809, 68HC05, 68HC11, 6301, 6309, 64180, Z80, Z180, 8085, and NSC800 μPs. You can configure the trace memory to capture as many as 8000 48-bit words or 4000 96-bit words, and you can set as many as 256 hardware breakpoints. The emulator can address as much as 16M bytes of memory, and it supports paged-memory systems by emulating page breaks and by performing page housekeeping functions. When debugging a target system, you can monitor target processor registers and various other system parameters during program execution. The emulator operates with any host computer or PC. You can obtain terminal-emulation and program-development software that runs on a PC for use with the emulator.

From $10,000.

Pentica Systems Ltd, Oakland Park, Wokingham, Berkshire RG11 2FE, UK. Phone (0734) 792101. TLX 848210.

Circle No 411

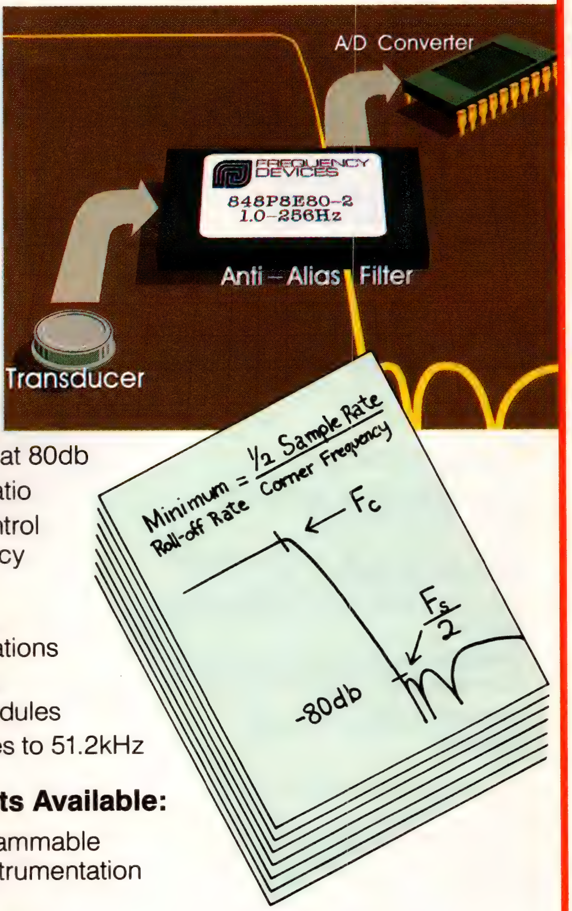
Pentica Systems Inc, 1 Kendall Square, Suite 2200, Cambridge, MA 02139. Phone (617) 494-1253.

Circle No 412

FILTER DESIGNER

- *Lets you design FIR and IIR digital filters*
- *Uses 64-bit floating-point arithmetic in calculations*

Filter Design and Analysis System (FDAS) version 1.2 lets you design lowpass and highpass IIR (infinite impulse response) filters with as



Programmable Anti-Alias Filters for Critical A/D Prefiltering

848P8E Series are Elliptic lowpass filters providing extremely sharp roll-off for A/D prefiltering.

Features:

- 8 pole, 6 zero elliptic lowpass filters
- Digitally programmable corner frequency
- Shape factor of 1.77 at 80db
- 8 bit (256:1) tuning ratio
- Internally latched control lines to store frequency selection data
- Ideal for single or multi-channel applications
- Plug in, ready to use, fully finished filter modules
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Other Filter Products Available:

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For more information about how Frequency Devices can meet your most critical filtering requirements, call our applications engineers at **(617) 374-0761.**

FREQUENCY DEVICES™
25 Locust Street
Haverhill, MA 01830
(617) 374-0761

CIRCLE NO 132

many as 40 poles, bandpass and bandstop IIR filters with as many as 80 poles, FIR (finite impulse response) windows with as many as 1024 poles, and Parks-McClellan FIR filters with as many as 256 poles. The transformation methods comprise bilinear and impulse-invariant transformations. The program uses 64-bit floating-point arithmetic for all calculations; you can vary the coefficient quantization from 8 to 32 bits to suit the word lengths of various digital-signal-processor ICs. Menu-driven screens and extensive error checking make the program easy to use. To run the program, you need an IBM PC/XT, PC/AT, PS/2, or a compatible machine having at least 640k bytes of RAM and 800k bytes of available hard-disk storage. The vendor recommends that you use MS-DOS version 3.1, but the program will run under version 2.0 or later. $495.

Momentum Data Systems Inc, 1666 Newport Blvd, Suite 115, Costa Mesa, CA 92627. Phone (714) 548-3257.

Circle No 413

MATH TOOL

- *Lets you perform complex mathematical analyses*
- *Runs on Macintosh II, Plus, and SE computers*

Eureka: The Solver is a mathematical tool that lets you use your Macintosh to solve a wide variety of mathematical problems, including simultaneous linear equations in multiple variables. You enter an equation in the text-editor window, and the program searches for the variables and finds a solution. You can then verify the solution, plot it, or send a report to the printer or to a disk file. The program can use the Macintosh II's 60881 math coprocessor and color capabilities. $195.

Borland International Inc, 4585 Scotts Valley Dr, Scotts Valley, CA 95066. Phone (408) 438-8400. TLX 172373.

Circle No 414

MATH LIBRARY

- *Mathematical and statistical Fortran routines*
- *Available in object form or transportable source code*

The Scientific Desk Library is a set of mathematical and statistical callable subroutines written in Fortran. They are available either in source-code or in an object-code format compiled for any one of a wide variety of computers, including IBM System/370; DEC VAX; IBM PC, PC/XT, PC/AT, PS/2, and RT PC families; Sun workstations; and Apple Macintosh. The routines in-

ANOTHER FIRST FROM PULSE

The New 3270 Line Interface
For "Type A" Coax

Pulse's module design reduces to a single component all transmission and receive signal conditioning, line coupling circuitry and the required isolation transformer functions.

PERFORMANCE ADVANTAGES:
- COMPACT PACKAGE—1/3rd the PCB Space of Discrete Circuit.
- LASER TRIMMED FOR ANALOG MATCHING AND TIGHT TOLERANCES—Aids in Zero Crossover Detection and Increased Noise Margins.
- LOWER INSTALLED COST—Single Device Eliminates 12 Component Insertions.
- ISOLATION 700 Vrms—For Safe Operation.

The modules are designed to be the only analog interface required between IBM 3270/3299 protocol emulating semiconductors and the transmission medium. Until now, this function was achieved using Pulse transformers and various additional components.

Our experience with millions of 3270 isolation transformers is combined with many years of thick film technology to provide a new generation of Specific Application Modules—SAM™

Comparison Table

	Manufacturer P/N	Pulse P/N
National Semiconductor	BCP8344V	PE-857623
Chips and Technologies	82C570	PE-857621
Standard Microsystems	COM 9004/9064	PE-857621

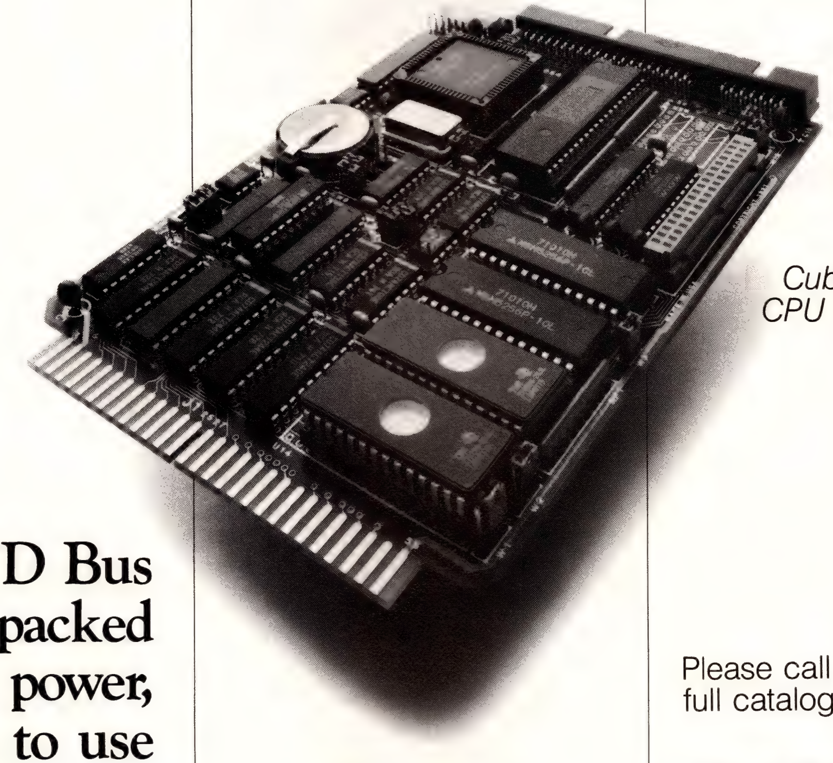
Call our applications engineers or your nearest sales office for samples, technical support, data sheets or design/applications assistance.

Pulse™
Pulse Engineering, Inc.
P.O. Box 12235 San Diego CA 92112
(619) 268-2400

CIRCLE NO 133

WHY STD BUS ?

- **V40 PROCESSOR RUNS AT 7.4 MHz**
- **8088 CODE COMPATIBLE**
- **ALL CMOS**
- **64K BATTERY-BACKED RAM**
- **128K EPROM**
- **TWO RS-232/RS-485 LINES**
- **THREE 8-BIT PARALLEL PORTS**
- **BATTERY-BACKED CLOCK-CALENDAR**
- **SBX CONNECTOR**
- **8-BIT, 8-CHANNEL A/D CONVERTER**
- **DEBUG FIRMWARE LINKS TO PC**



Cubit's Model 8400 CPU Board - $490

STD Bus
is packed
with power,
simple to use
and costs less
than VME
or Multibus®.

Please call or write for our full catalog.

CµBIT DIVISION OF PROTEUS INDUSTRIES

190 South Whisman Road
Mountain View, CA 94041-1577
Telephone: (415) 962-8237

Multibus® is a registered trademark of Intel Corp.

CIRCLE NO 134

EDN NEWS

Memory Boom by Mid-1990

Military Gate Arrays

EDN NEWS

Low-Cost Spectrum Analyzer

Reflectometer Isolates LAN Faults

EE Education Gets A Boost in New Jersey

NEWSBRIEFS

DSP Board Fits IBM PC

Power MOSFET Makers Boost Electrical Specs

INSIDE

The Temptations of Temping

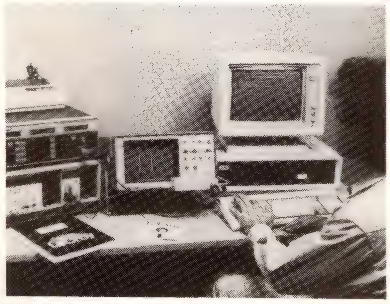
HOT NEWS OF PRODUCTS, TECHNOLOGY, AND CAREERS

EDN NEWS

clude arithmetic; elementary and special functions of mathematical physics; linear algebra; optimization; nonlinear equations; differential equations; integral transforms; statistics and probability; and error analysis. The annual license fee of $1500 includes maintenance, consultation, and the automatic forwarding of augmented versions.

C Abaci Inc, 208 St Mary's St, Raleigh, NC 27605. Phone (919) 832-4847.

Circle No 415



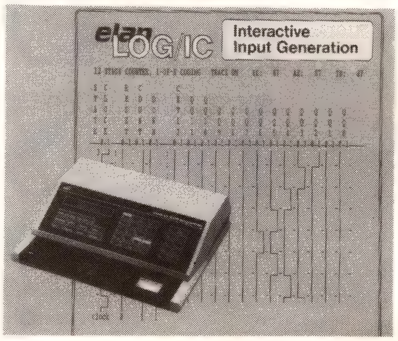
CALIBRATION SOFTWARE

- *Checks specifications of the 9400 digital oscilloscope*
- *Reference parameters traceable to NBS standards*

The CS01 calibration software package runs on an IBM PC or a compatible computer equipped with a math coprocessor and an IEEE-488 interface from National Instruments. The program performs an extensive series of tests that verify the performance specifications of the vendor's 9400 digital oscilloscope; some of these tests require the use of high-quality external signal generators. The software allows you to test individual specifications with computer assistance or to perform an automated calibration check. If you use signal sources traceable to a standard, the calibration will be traceable to the same standard. The package includes a computer-aided adjustment procedure that guides a trained technician through the steps that are needed to correct the settings of the 9400 so that the performance of the instrument meets all the specifications. $1200. Delivery, eight weeks ARO.

LeCroy Corp, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 578-6084. TWX 710-577-2832.

Circle No 416



LOGIC SIMULATOR

- *High-level-language constructs*
- *Displays simulation results as on-screen logic waveforms*

Running on the DEC VAX or IBM PCs and compatibles, this functional verifier enhances the company's LOG/IC logic design compiler. Providing both logic verification and simulation, the package features interactive user input and high-level-language constructs—for example, If-Then-Else, Do-While, and For-End-For instructions. The interactive user interface allows you to modify and resimulate logic circuits without having to create new binary input information. The inputs and outputs are displayed as waveforms on the screen in a format similar to that provided by a logic analyzer. You can breakpoint inputs or outputs and trace as many as 1024 simulated states. £730 for IBM PCs and compatibles; £2200 for the DEC VAX.

Elan Digital Systems Ltd, 16-20 Kelvin Way, Crawley, West Sussex RH10 2TS, UK. Phone (0293) 510448. TLX 877314.

Circle No 417

Elan Digital Systems, 2162B N Main St, Walnut Creek, CA 94596. Phone (415) 932-0882.

Circle No 418

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Allen-Bradley has been making rugged Variable Resistors since the 1930's. Our quality was good then. It's *excellent* now. While we have one of the broadest lines of standard panel and trimming potentiometers in the industry ... Allen-Bradley's strength is in our ability to *customize* pots to suit your particular applications with special tapers, shafts and much more. We can accommodate your needs with a reliable unit at a reasonable cost.

Our hot-molded, heavy-duty Type J Panel pot continues to be the standard in the industry for tough applications and high power capabilities. Single, dual and triple sections are available in a wide resistance range (to 5 Megohm). It's simply the best in the business.

Our Type W compact hot-molded pots are available in a metal or all plastic housing. We customize these reliable pots to suit you and your application needs. W pots provide high performance panel control with lug or PC terminals and a wide resistance range (to 5 Megohm).

Allen-Bradley covers the spectrum ... in variety, styles and products with only one standard of quality ... *superior.*

For more information, call:
1-800-592-4888 or **1-800-292-4888** (in Texas)
Or write for Publication ROPP
Allen-Bradley
1414 Allen-Bradley Dr.
El Paso, TX 79936-6414

A·B QUALITY
ALLEN-BRADLEY
A ROCKWELL INTERNATIONAL COMPANY

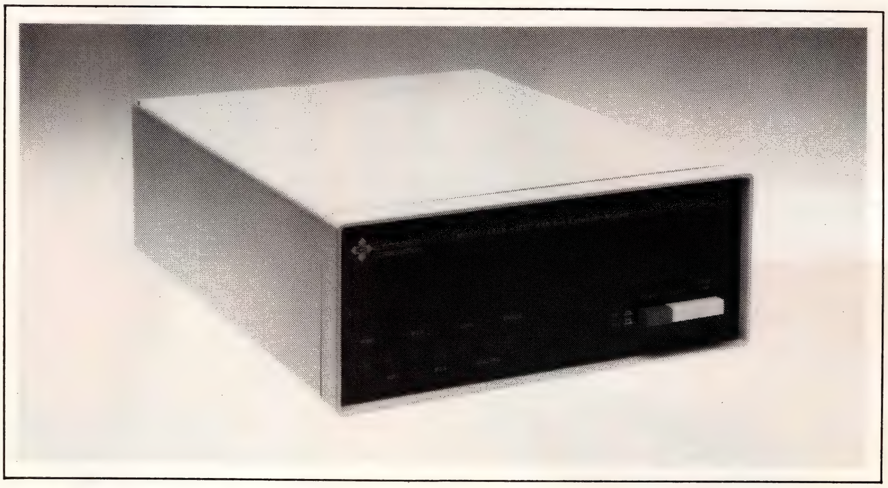
CIRCLE NO 135

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

IEEE-488 EXTENDER

- *Includes 300/1200/2400 bps modem*
- *Controls IEEE-488 devices over dial-up phone lines*



Model 4888, an IEEE-488 bus extender, contains a 300/1200/2400-bps modem to allow control of instruments and other bus-oriented devices over dial-up telephone lines. Except for the response delay that occurs during parallel polling, the bus operates as if the devices were adjacent to the controller; your computer can call remote sites to collect data or command actions and remote instrumentation can "call home" to warn of abnormal conditions. The modem is compatible with CCITT V.22 bis, V.22/V.21, and Bell 212/103 protocols. The unit compresses data to minimize message length, and its firmware includes error-correction and -diagnosis routines. Its integral memory saves the last number dialed and stores a directory of 32 numbers. $1895.

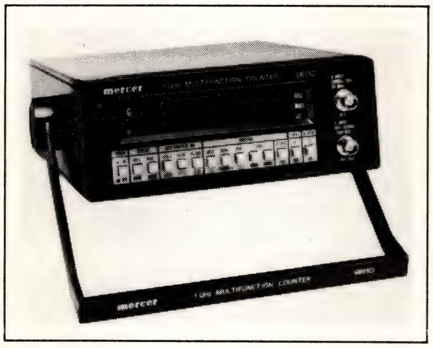
ICS Electronics Corp, 2185 Old Oakland Rd, San Jose, CA 95131. Phone (408) 432-9009. TLX 286895.
Circle No 420

IN-CIRCUIT EMULATORS

- *Emulate 80286 and 80C186 at 12.5 MHz*
- *Feature 128k bytes of 0-wait-state mappable RAM*

The Ice-286 and -186 in-circuit emulators support the vendor's 80286 and 80C186 (a CHMOS version of the 80186) µPs at clock rates as high as 12.5 MHz with zero wait states. The emulators are hosted by an IBM PC/AT or compatible computer; their trace buffers can capture 2048 data frames, including both execution and data-bus activity. The zero-wait-state emulation memory for each unit totals 128k bytes. You can map the I/O addresses anywhere within the emulation memory, in 4k-byte increments. The vendor furnishes a symbolic debugger with the units; you can debug code developed in PL/M, Pascal, Fortran, and C. Ice-186, $9995; Ice-286, $12,495.

Intel Corp, Box 58065, Santa Clara, CA 95052. Phone (408) 987-8080. **Circle No 421**



FREQUENCY COUNTERS

- *Cover 10 Hz to 100 MHz and 10 Hz to 1 GHz*
- *Provide 8-digit LED display*

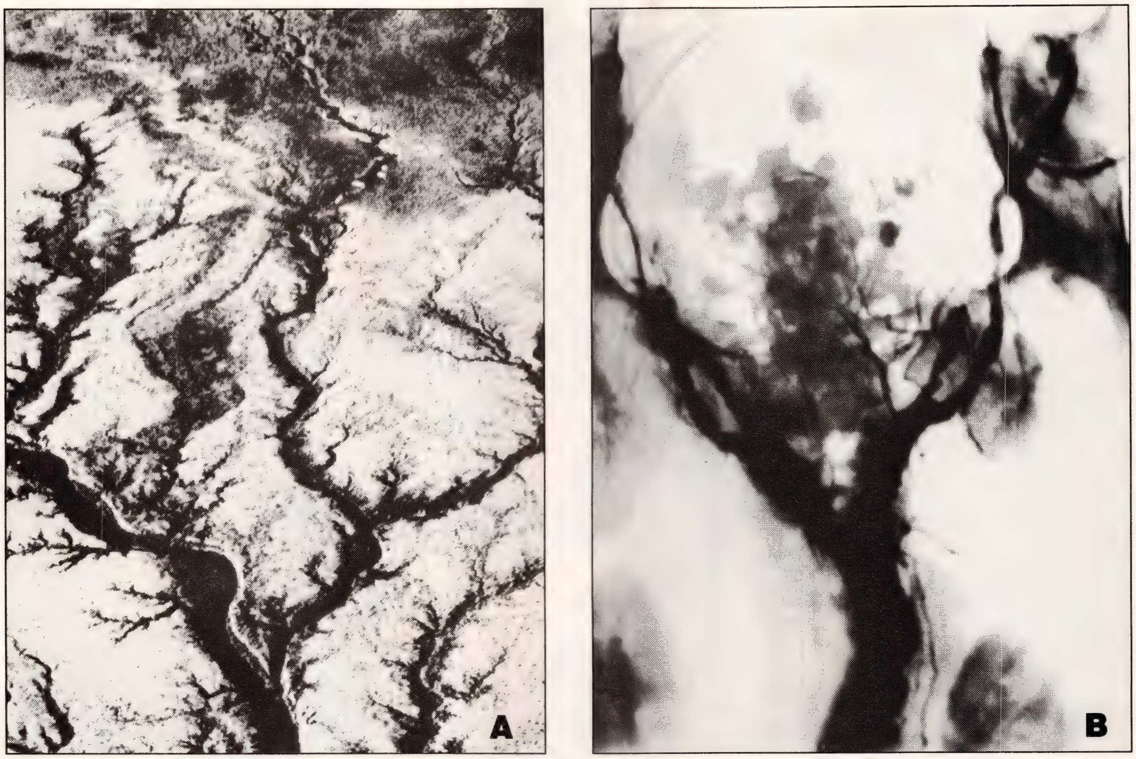
Sporting reference ovens that hold timebase temperature coefficients to $\pm10^{-6}$ from 0 to 40°C and offering timebase aging of $\pm3\times10^{-7}$/month, the 9800 and 9810 frequency counters cover 10 Hz to 100 MHz and 10 Hz to 1 GHz, respectively. Eight 7-segment LED digits display the readings. All inputs to the counters occur via front-panel connectors. A 1-MΩ input provides sensitivity of 25 mV rms at 5 MHz and below, and of 50 mV rms from 5 to 100 MHz. The 9810 has a separate 50Ω input that accepts high-frequency signals from 15 mV rms to 3V peak. Above 10 MHz, the counters use a 10:1 prescaler to divide the input frequency. 9800, $255; 9810, $475.

Mercer Electronics, 859 Dundee Ave, Elgin, IL 60120. Phone (312) 697-2260. TLX 722416.
Circle No 422

SURGE TESTER

- *Supplies high-energy surges and makes surge measurements*
- *Includes 80386-based computer*

The System 2/XX is a family of high-speed, high-power surge testers for testing semiconductor surge protectors and protector arrays (for example, protected connectors). The vendor can also configure the products for testing power semiconductor devices such as rectifiers, transistors, power FETs, and SCRs. The systems can generate high-power surges, such as 8×20 µsec impulses at 500A peak or



Delta or Aorta? Which is Which?

No problem here because both of these images were processed on Raytheon's new TDU-850 Thermal Display Unit.

The TDU-850 is the only thermal recorder to display true grey levels (not mere halftone representations) at such high speeds and resolutions. Utilizing 203 dots per inch, the unit offers 64 grey levels and can provide 256 grey levels through the use of super pixels. The TDU-850 is your assurance of high quality images. Standard units about $5,000. (Slightly higher overseas). RS-170 video and IEEE-488 computer interfaces are available.

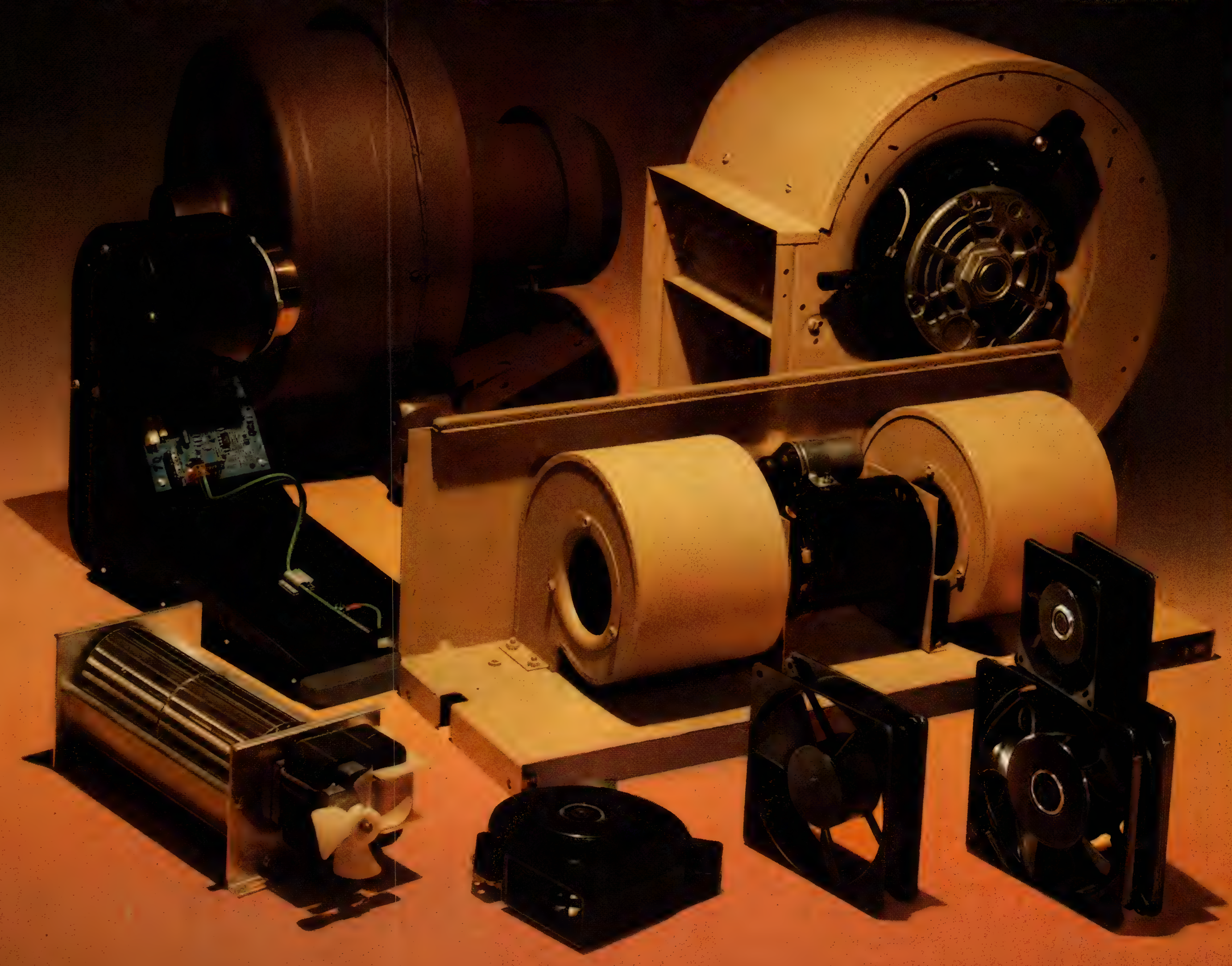
When you must know what you're looking at, look for equipment that knows what to look for. For details call or write **Marketing Manager, Recorder Products, Raytheon Company, Submarine Signal Division, 1847 West Main Road, Portsmouth, RI 02871-1087. Phone: (401) 847-8000.**

Raytheon

A. Satellite view of river delta. **B.** Arterial angiogram.

Note: These began as continuous tone images which were processed in black and grey by a TDU-850. The TDU-850 images, however, had to be converted to conventional halftones in order to be shown in this magazine. Thus the high quality of the original TDU-850 images have been obscured. For true results ask to see a demonstration.

MOVING AIR IS EASY



CONTROLLING IT TAKES AN EXPERT

With the TORIN line of blowers, FASCO specializes in creating solutions to air-moving problems. Over 50 years of experience has established our reputation for leadership in custom blower design. Applications include cooling for electronic, business machine, aerospace and military products.

Our design expertise covers single, dual and multi-stage centrifugal blowers, transverse-flow blowers, mixed-flow blowers, cabinet blowers, tube and vane-axial fans. We provide country-wide factory sales coverage, in-house availability of electric motors and cost-effective production capabilities.

Call on us when your air-moving requirements exceed the ordinary. Our product line is limited only by your imagination.

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MOTOR DIVISION HEADQUARTERS
500 Chesterfield Center
Suite 200
St. Louis, MO 63017
(314) 532-3505/Telex: 44-7455
Telecopy: (314) 532-9306

CIRCLE NO 137

10×1000 μsec impulses at 250A peak. Besides generating surges, the units measure the surge response of devices under test. For example, the units can measure the peak voltage that appears across a protective device and the current that flows through it. In addition, the testers make static measurements of device parameters such as forward and reverse leakage. The systems, which are hosted by Compaq 386 computers and interface to a variety of device handlers, store data on hard disk and incorporate streaming-tape drives for backup. $130,000 to $400,000. Delivery, six to 12 months ARO.

KeyTek Instrument Corp, 260 Fordham Rd, Wilmington, MA 01887. Phone (617) 658-0880.

Circle No 423

Z180/64180-Z EMULATOR

- *Does not slow target systems clocked at 8 MHz*
- *Hosted by ASCII terminal or computer*

You can control the Z180 Icebox from any terminal or computer with a bidirectional RS-232C port. The in-circuit emulator uses the target system's clock, whose speed may be as high as 8 MHz; using the emulator does not slow down the target system. The unit, which includes 64k bytes of overlay RAM mappable anywhere in the target's memory space, supports all features of the Z180 and 64180-Z including the memory-management unit, extended I/O addressing, and the processors' ability to address 1M byte of memory. You can set and clear as many as 64k hardware breakpoints in RAM and ROM individually and in regions. You can transfer code between a host computer and the emulator in Intel Hex format or as unformatted binary data; the vendor ships an assembler and disassembler with the unit. The emulator's firmware contains several routines that diagnose hardware faults in the target; you can invoke these routines with 2-letter commands. Emulator, $1395; emulator with support software and software performance analyzer, $3100.

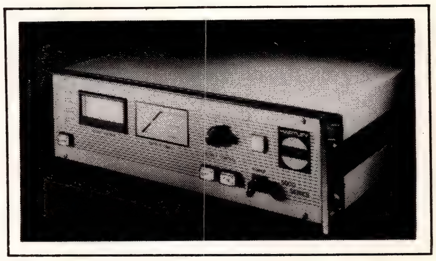
Softaid Inc, 8930 Rt 108, Columbia, MD 21045. Phone (301) 964-9455.

Circle No 424

CAPACITOR CHARGERS

- *Output circuitry minimizes stored energy*
- *Chargers include safety features to protect operators*

The Series 5000 capacitor chargers are available with maximum output-voltage ratings of 1 to 50 kV. They charge at a nominal rate of 200A; a 10-turn potentiometer lets you set the final charge-voltage level. A front-panel meter continuously monitors the capacitor voltage. The safety features include a load-dump switch (which you can operate via a front-panel pushbutton or via external safety-interlock switches); output short-circuit protection; and a key-operated power switch. Front-panel LEDs indicate the progress of the charging operation, the output polarity, output grounded conditions, and interlock status. Remote-control and monitoring facilities are also provided. £4000 to £7500 for 1- to 30-kV models; from £9000 for 40- and 50-kV models.



Hartley Measurements Ltd, Bear Ct, Daneshill E, Basingstoke, Hampshire RG24 0QT, UK. Phone (0256) 56695. TLX 858733.

Circle No 425

Find the small change:

2.19640	2.19640	2.19640	2.19640	2.19640
2.19640	2.19640	2.19640	2.19640	2.19640
2.19640	2.19640	2.19640	2.19640	2.19640
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2.19640	2.19640	2.19640	2.19640	2.19640
2.19640	2.19640	2.19640	2.19640	2.19640
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2.19640	2.19640	2.19640	2.19640	2.19640
2.19640	2.19640	2.19640	2.19640	2.19640
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2.19640	2.19640	2.19640	2.19640	2.19640
2.19640	2.19640	2.19640	2.19640	2.19640
2.19640	2.19640	2.19640	2.19640	2.19640
2.19640	2.19640	2.19640	2.19640	2.19640

The 197 Microvolt DMM detects the small change—one part in 220,000—for small change: $620. And you can automate with its IEEE-488 option. Find out how to get a big change in your measurement capabilities. Call the Keithley Product Information Center: (216) 248-0400.

The Model 197 Microvolt DMM

KEITHLEY

CIRCLE NO 138

Who manages the power in GAI's MATE 390 Hybrid Automatic Test Systems?

KEPCO POWER MANAGERS™

For many years, Giordano Associates, Inc. has manufactured commercial factory functional test equipment in support of major military and commercial test equipment. Their new line of Air Force MATE compatible equipment, designated the MATE 390 Test System, was created as part of their continuing effort to be completely responsive to the needs and requirements of ATLAS 716 based systems. It integrates commercially available programmable test instruments into a modular functioning test system that will deter obsolescence.

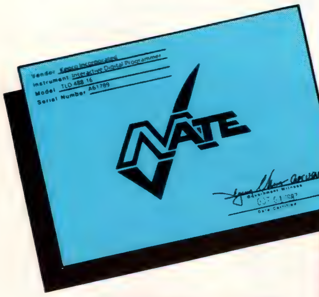
From the beginning, Kepco Power Managers programmed by Kepco Digital Interfaces have supplied the controlled power in GAI systems. And, says GAI's Automation Division president, Al Esser, "Kepco's proven track record in the Air Force's MATE System arena, and its past record in GAI Test Systems, make Kepco programmable power supplies the natural choice for use in GAI's new line."

In the MATE 390 System shown here, four Kepco Series ATE Power Managers are controlled by a Kepco MATE Verified* TLD 488-16 Interactive Programmer.

The Kepco Power Managers are linear power supplies that have been designed specifically for programming applications. They stabilize voltage to 0.001% and current to 0.005%, respond to programming step inputs in microseconds, and will deliver maximum rated voltage *and* current simultaneously.

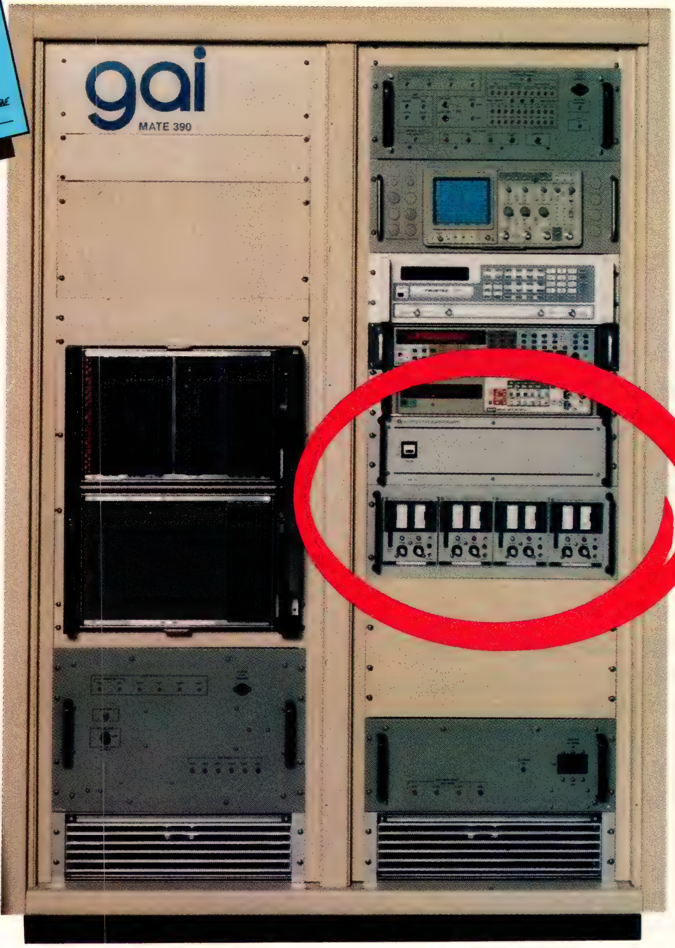
The Kepco TLD 488-16 commands, *and reacts to responses from,* up to 16 Kepco Power Managers at once through a single GPIB address. It communicates with GAI's computer in the Control Interface Intermediate Language (CIIL), over their IEEE-488 bus. The responses it receives from the power supplies under its control tell it whether they have obeyed its commands, and if not, why not. When combined with Kepco Power Managers, the TLD 488-16 gives GAI the most precise, the most flexible control of power available today.

Can we manage the power in your systems?



Vendor Kepco Incorporated
Instrument Interactive Digital Programmer
Model TLD 488 16
Serial Number A61789
Government Witness
OCT 01 1987
Date Certified

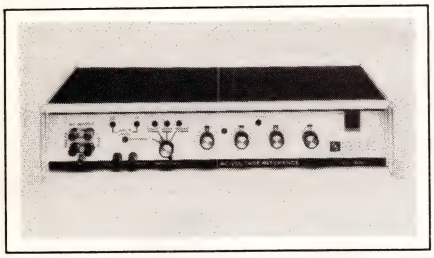
*On October 1, 1987 Kepco's TLD officially achieved "MATE-verified" status. The certificate shown was issued by the MATE program office, Kelly AFB, Texas.



Call or write:
Dept. KSF-12,
KEPCO, INC.,
131-38 Sanford Avenue,
Flushing, NY 11352 USA
(718) 461-7000
TWX #710-582-2631
FAX (718) 767-1102.

KEPCO.
THE POWER SUPPLIER™

CIRCLE NO 141



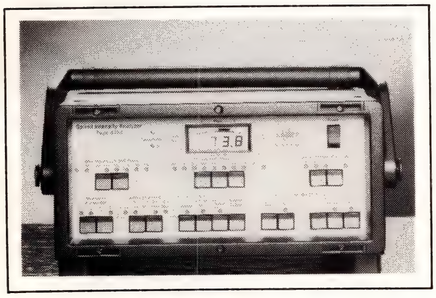
AC CALIBRATOR

- *Covers 50 to 400 Hz*
- *Output rms voltage is within 0.06% of setting*

The 4032 calibrator provides an ac voltage of as much as 10V rms that is accurate to within 0.06% of setting; its harmonic distortion doesn't exceed 0.03%. The unit's output frequency ranges from 50 to 400 Hz. The instrument generates 50, 60, and 400 Hz internally and provides terminals to which you can connect an oscillator that produces other frequencies. The rack-mount unit is 3.5 in. high and weighs 8 lbs. $945.

Electronic Development Corp, 11 Hamlin St, Boston, MA 02127. Phone (617) 268-9696.

Circle No 426



SOUND METER

- *Performs in situ measurements even in high ambient noise*
- *Discriminates between different sound sources*

The Model 4433 sound-intensity analyzer's 2-microphone pressure-gradient technique lets you take measurements in situ that you would normally have to take in an anechoic room. The technique allows the instrument to locate and discriminate between different sound sources to provide you with a complete acoustic picture, even in environments with high ambient-noise levels. The instrument has sound-intensity, particle-velocity, and sound-pressure measurement modes. It also performs automatic sequential-octave analysis, A-weighted and linear analysis, and linear or exponential averaging. The instrument features autoranging and provides an indication of noise impulses that exceed the selected range. It is battery powered. You can obtain software that permits you to postprocess measurements on a Hewlett-Packard personal computer or on an IBM PC or compatible computer. With a Model 3520 sound probe, $11,950.

Bruel & Kjaer, Hovedgade, 2850 Naerum, Denmark. Phone (2) 800500. TLX 37316.

Circle No 427

Bruel & Kjaer Instruments Inc, 185 Forest St, Marlborough, MA 01752. Phone (617) 481-7000. TWX 710-347-1187.

Circle No 428

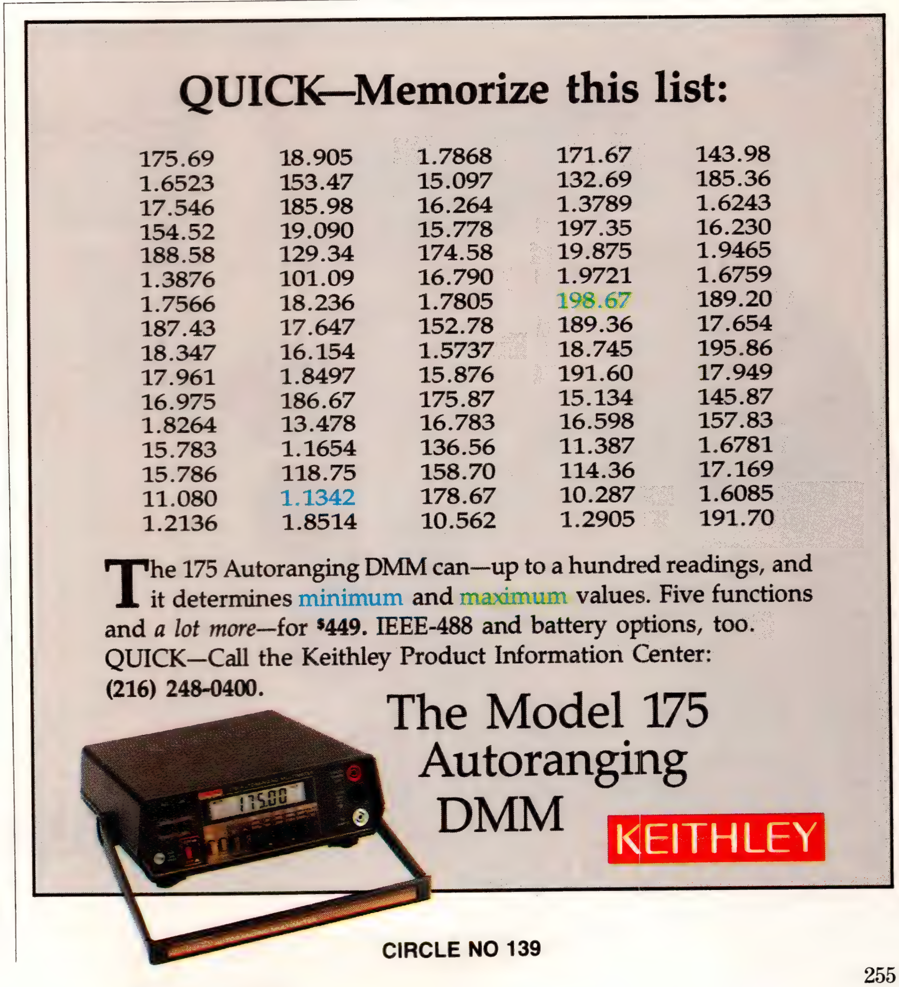
EPROM EMULATOR

- *Emulates 2716 through 27256*
- *Features battery-backed RAM*

The ROMX-2 emulates EPROMs in the 2716 through 27256 series. It contains 64k bytes of battery-backed RAM; you can also order it with 256k bytes as an option. Unlike EPROM data, which you can't easily change, data in the emulated EPROM is easy to change. As with EPROMs, you can remove power from the target system without losing data and without damaging the emulator. The unit accepts data as ASCII characters through its RS-232C port or in Intel hex format at rates of 1200 to 19,200 bps. You can use multiple emulators with a target system that has a 16- or 32-bit-wide ROM memory. $399.

Gtek Inc, Drawer 1346, Bay St Louis, MS 39520. Phone (601) 467-8048. TLX 315814.

Circle No 429



QUICK—Memorize this list:

175.69
1.6523
17.546
154.52
188.58
1.3876
1.7566
187.43
18.347
17.961
16.975
1.8264
15.783
15.786
11.080
1.2136
18.905
153.47
185.98
19.090
129.34
101.09
18.236
17.647
16.154
1.8497
186.67
13.478
1.1654
118.75
1.1342
1.8514
1.7868
15.097
16.264
15.778
174.58
16.790
1.7805
152.78
1.5737
15.876
175.87
16.783
136.56
158.70
178.67
10.562
171.67
132.69
1.3789
197.35
19.875
1.9721
198.67
189.36
18.745
191.60
15.134
16.598
11.387
114.36
10.287
1.2905
143.98
185.36
1.6243
16.230
1.9465
1.6759
189.20
17.654
195.86
17.949
145.87
157.83
1.6781
17.169
1.6085
191.70

The 175 Autoranging DMM can—up to a hundred readings, and it determines minimum and maximum values. Five functions and *a lot more*—for $449. IEEE-488 and battery options, too. QUICK—Call the Keithley Product Information Center: **(216) 248-0400.**

The Model 175 Autoranging DMM

KEITHLEY

CIRCLE NO 139

More Functions. Smaller Budget.

Beckman Industrial Circuitmate™ DMMs put hFE, Logic, Capacitance, Frequency and True RMS In Your Hand. For Less.

Get more, for less. It's a simple definition of value. For DMMs, value means finding the combination of capabilities that meets your needs at the right price. Without losing sight of accuracy and reliability. If you want more functions at a low price, Beckman Industrial's Circuitmate™ Digital Multimeters are the best value around.

From the pocket-sized DM20L to the DM850, with true RMS capability and accuracy to 0.05% ±1 digit, Circuitmate DMMs give you the functions you need.

For instance, the DM20L puts both a Logic Probe, a transistor gain function (hFE), and a full range of DMM functions in the palm of your hand. For only $79.95.

Then there's the DM25L. Where else does $99.95 buy you a Logic Probe, capacitance measurement, transistor gain function (hFE), and 24 DMM ranges including resistance to 2000 megohms? Nowhere else.

When high accuracy counts, there's the DM800 with a 4½ digit display. The DM800 also gives you frequency counting. A full-function DMM, and more, doesn't have to cost over $195.00. If it's a Circuitmate DM800.

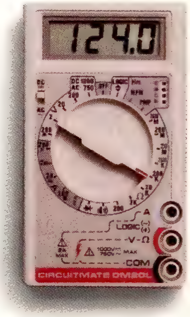
Or, for a few dollars more, get true RMS (AC coupled) to let you accurately measure non-sinusoidal AC waveforms, and all the capability of the DM800, in the DM850.

Of course, there's a whole range of Circuitmate DMMs and service test instruments, including the DM78 autoranger that fits in a shirt pocket, yet gives you a full size 3½ digit, ⅜" readout. Not to mention a complete line of accessories like test leads, current clamps, even probes that can extend your DMMs range and sensitivity. All designed to work flawlessly with your Beckman Industrial Circuitmate DMM.

EMERSON

DM20L Pocket-Size w/Logic $79.95*

- TTL Logic Probe: 20MHz Hi/lo/off indications Detects 25nS pulse widths
- hFE (NPN or PNP): 1 range (1000)
- DMM: Input Impedance—10 Megohms DCA/ACA-5 ranges (200μA to 2A)
- Ohms-8 ranges (200 ohms to 2000 Megohms)
- Continuity beeper



DM850 True RMS

- 4½ digits. DCV accuracy is .05% +3 digits
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- Anti-skid pads
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- *Levels are programmable from −70 to 20 dBm*
- *Meets spec 150 msec after a level change*

The 2520 RF calibrator produces an NBS-traceable 30-MHz output at levels from −70 dBm to 20 dBm with 0.1 dB resolution. At 0 dBm, the maximum error is ±0.055 dB. The instrument, which is programmable from its front panel and from an IEEE-488 interface, meets all requirements of MIL STD-28800C, type II, class 5. Its front-panel alphanumeric display with cursor controls provides status and output-level indications. The unit's output meets its accuracy specifications within 150 msec after you command it to change. The output impedance is 50Ω with VSWR of <1.05. The vendor ships the unit with a 75Ω adapter. When you use the adapter, the output automatically adjusts to correct for impedance mismatch. $2250. Delivery, 12 weeks ARO.

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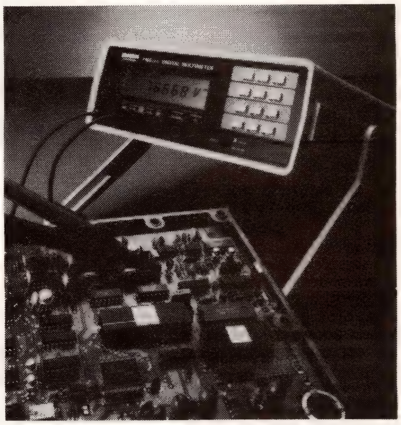

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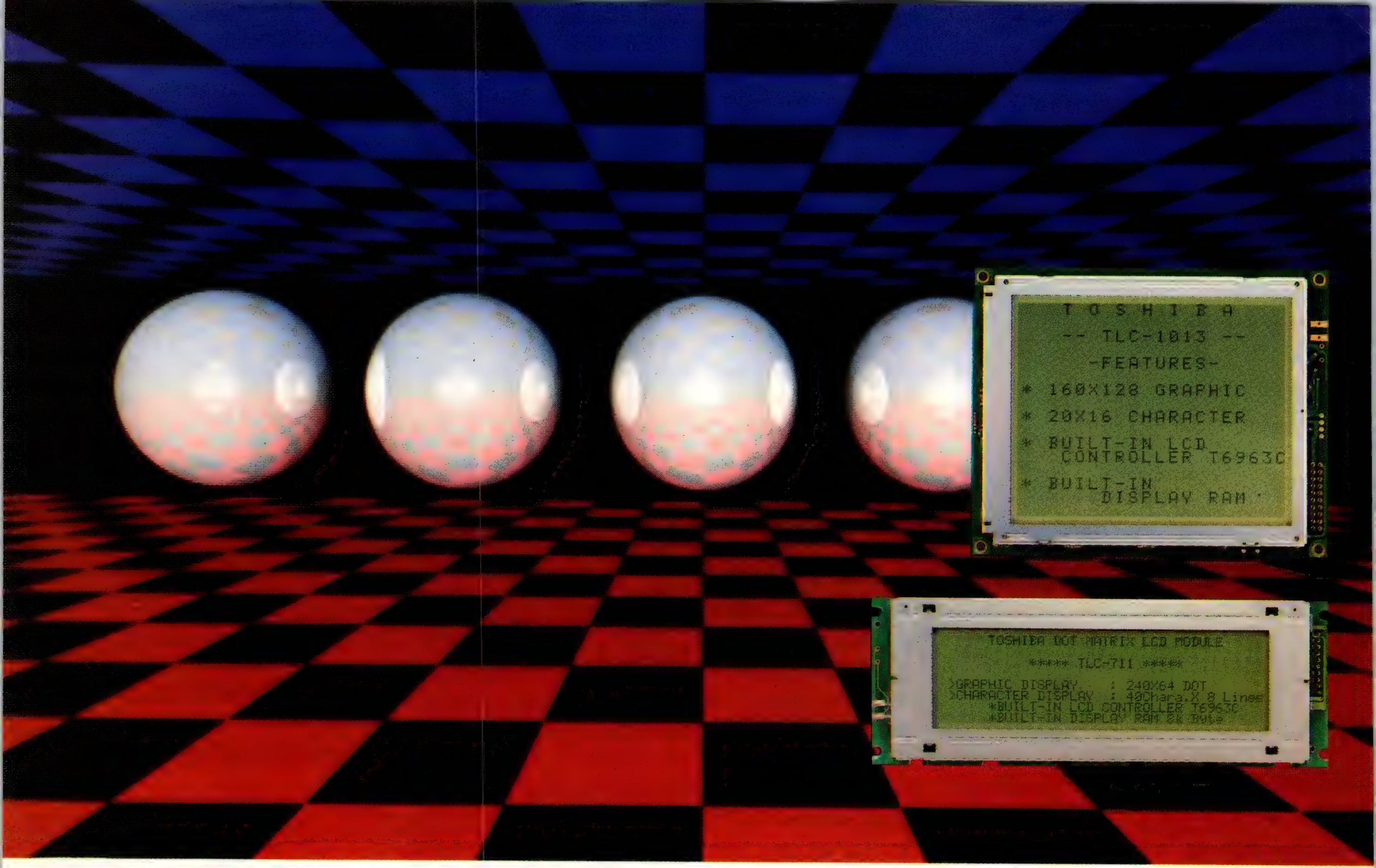
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TLC-731	16 × 4	87.0 × 60.0 × 12.0
TLC-501	20 × 2	116.0 × 37.0 × 12.5
TLC-721	20 × 4	98.0 × 60.0 × 12.0
TLC-691	24 × 1	126.0 × 36.0 × 12.0
TLC-771	24 × 2	118.0 × 36.0 × 12.0
TLC-601	40 × 1	182.0 × 33.5 × 13.0
TLC-591	40 × 2	182.0 × 33.5 × 13.0
TLC-1001	40 × 4	221.0 × 76.0 × 12.5

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TLC-711A	240 × 64	180.0 × 65.0 × 12.0	T6963C
TLC-1013	160 × 128	129.0 × 104.5 × 14.0	T6963C
TLC-1091	240 × 128	241.0 × 125.3 × 12.0	T6963C
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TLC-341AK	128 × 128	93.2 × 86.6 × 12.0	(T6963C)
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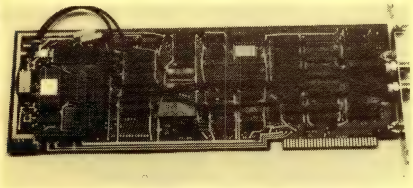

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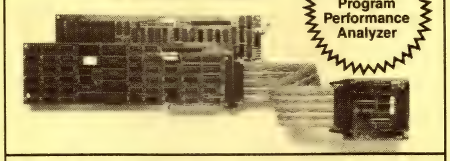

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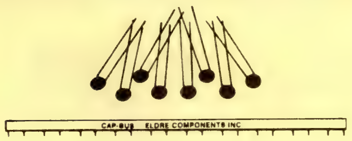

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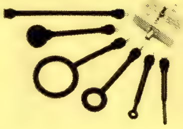

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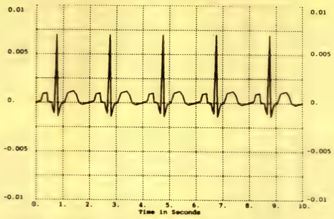

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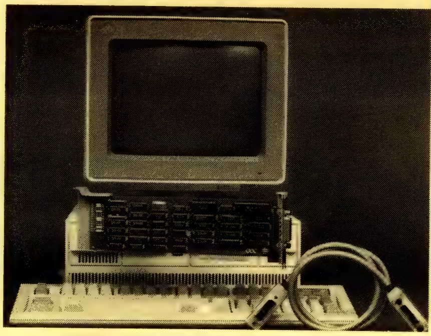

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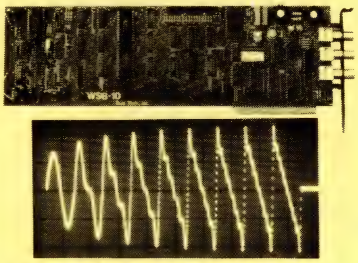

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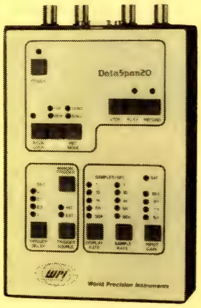

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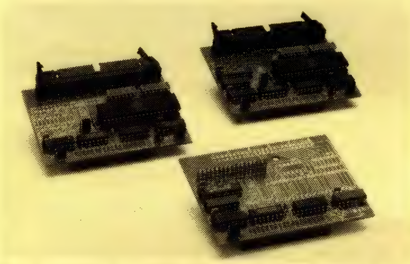

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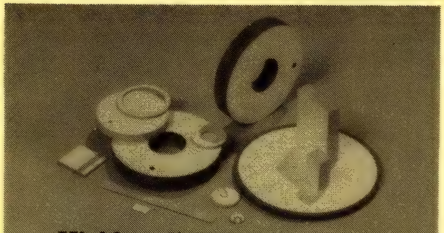

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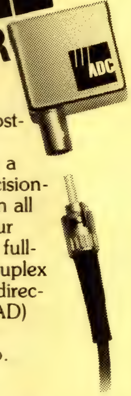

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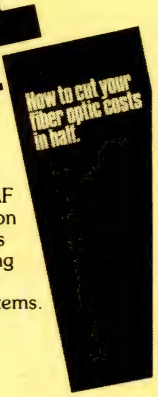
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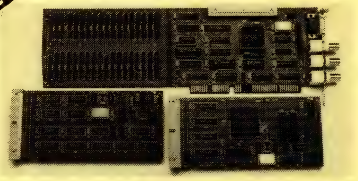

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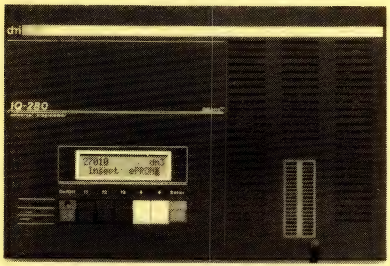

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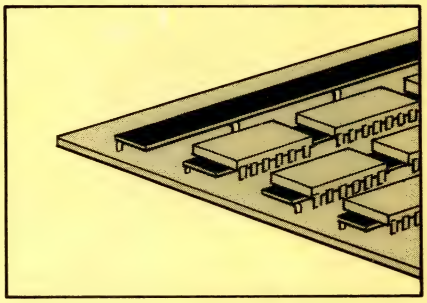

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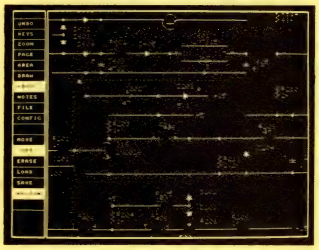

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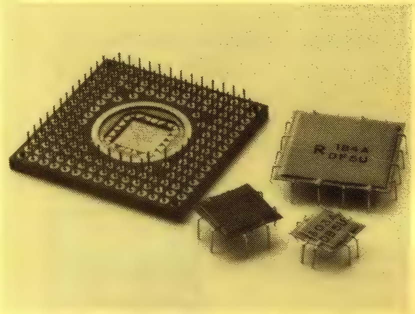

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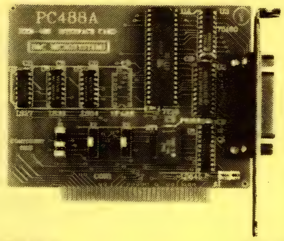

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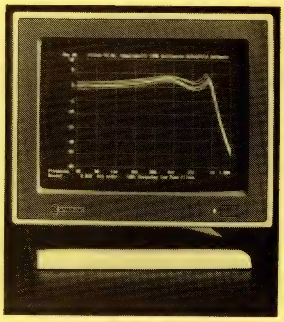

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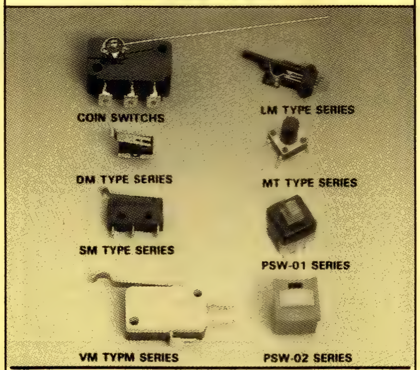

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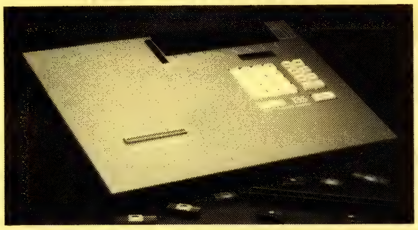

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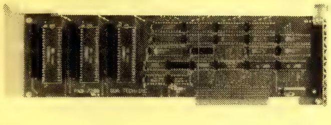

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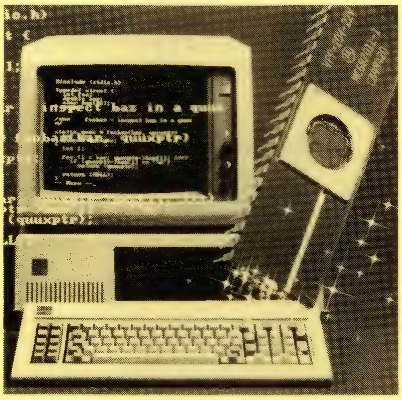

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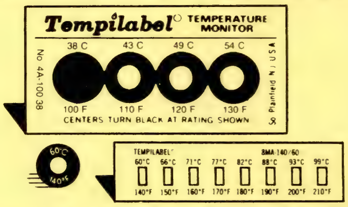
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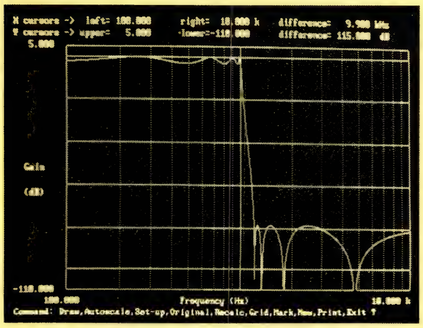

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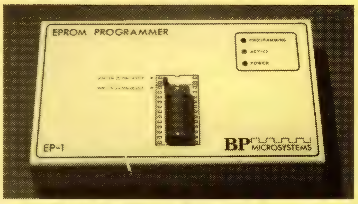

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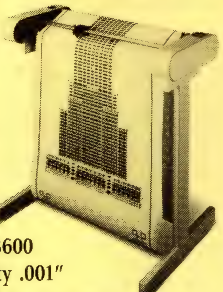

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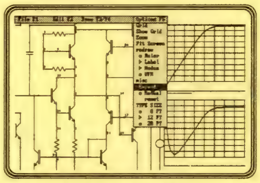

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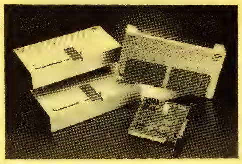

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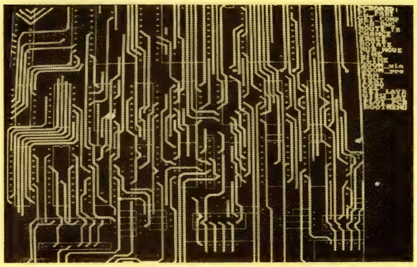

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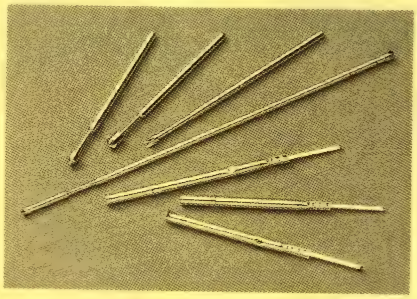

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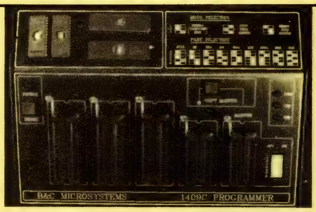

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Brochure summarizes emulator's capabilities

This 4-pg brochure describes how the vendor's in-circuit emulator provides development-system support for 68000 CPUs. It focuses on the Ice-Engine/68K stand-alone product that you can use with PCs, host computers, or dumb terminals. The publication provides system configurations and block diagrams in schematic form, as well as a summary of commands.

Ziltek Corp, 1651 E Edinger Ave, Santa Ana, CA 92705.

Circle No 435

8-channel recorder described

This 8-pg booklet describes the Model MT-8800 8-channel direct-writing recorder. It presents chart samples of a variety of real-time modes, including eight 20-mm channels and full-scale overlapping waveforms. It also contains charts that demonstrate data captured by a trigger or by an on-demand snapshot. Finally, the publication reports on the vendor's family of signal conditioners and provides a complete list of specifications for the recorder.

Astro-Med Inc, Astro-Med Industrial Park, West Warwick, RI 02893.

Circle No 436

The human side of programming

In the 20-pg booklet *Experts' Views on the Human Interface Traits of Successful Commercial Software*, programmers discuss the importance of interaction with users during program development, as well as the need to provide accessible software. Rather than developing an impersonal flow chart, they emphasize that programmers should consider users' personalities, demands, and work styles. The document includes interviews with each programmer in question and answer format. Finally, the reference section gives brief descriptions of books, publications, and organizations devoted to the human side of software development.

Solution Systems, 541 Main St, South Weymouth, MA 02190.

Circle No 437

Volume 4 added to WCA handbook series

Volume 4, the latest addition to the worst-case circuit analysis (WCA) handbook, covers worst-case testing of electronic circuits and systems. Each chapter in the book deals with different circuit technology—that is, analog, digital, and power-conversion circuits; and RF and microwave devices and circuits. Test descriptions include detailed block diagrams of test setups, theory of operation, step-by-step test procedures, examples of typical test results, and a discussion of those areas where you must take special care to ensure the accuracy and repeatability of test data. The material is organized by circuit type and test parameter. 4-volume set, $680. You may also purchase a volume separately.

Design and Evaluation Inc, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043.

INQUIRE DIRECT

Journal for Macintosh users

The CAD/CAM Journal for the Macintosh Professional surveys Macintosh advancements in computer-aided design and computer-aided manufacturing. The publication covers the expanding field of CAD/CAM/CAE applications and features stories about evaluations of 2D and 3D drafting and design software, communications and CAD, hardware evaluations, and the most recent CAD/CAM/CAE products. $20 (six issues).

The CAD/CAM Journal, 16 Beaver St, New York, NY 10004.

INQUIRE DIRECT

Listing of IEEE and data-acquisition devices

The 1988 catalog *IEEE-488 Control, Data Acquisition and Analysis for Your Computer* contains information about all of the vendor's IEEE-488 products, as well as software and supporting hardware products for data acquisition, data reduction, data analysis, and data presentation. It lists recently introduced hardware devices, such as the MC-GPIB interface for the PS/2 and three MicroGPIB products. An integrated software system, LabWindows, completes the roster of latest products.

National Instruments, 12109 Technology Blvd, Austin, TX 78727.

Circle No 438

EDN's CHARTER

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EDN covers new and developing technologies to inform its readers of practical design matters that will be of concern to them at once or in the near future.

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Deborah Asbrand, *Associate Editor*

Ability—not disability—makes the engineer

Meet an engineer-to-be, a practicing engineer, and a retired engineer who explain why other people's attitudes are sometimes their greatest obstacle.

Ralph Arnold is on his way to becoming an engineer's engineer. A lifetime devotee of electronics, Arnold was already a veteran of many Heathkit projects when he entered high school in 1963. He studied electronics through an RCA correspondence class, and, as a junior and senior, attended extracurricular sessions for students who excelled in science and technology. His senior project was the design and assembly of a computer that used discrete-transistor logic—a goal that was impossible for a high-school senior, but one that he pursued anyway.

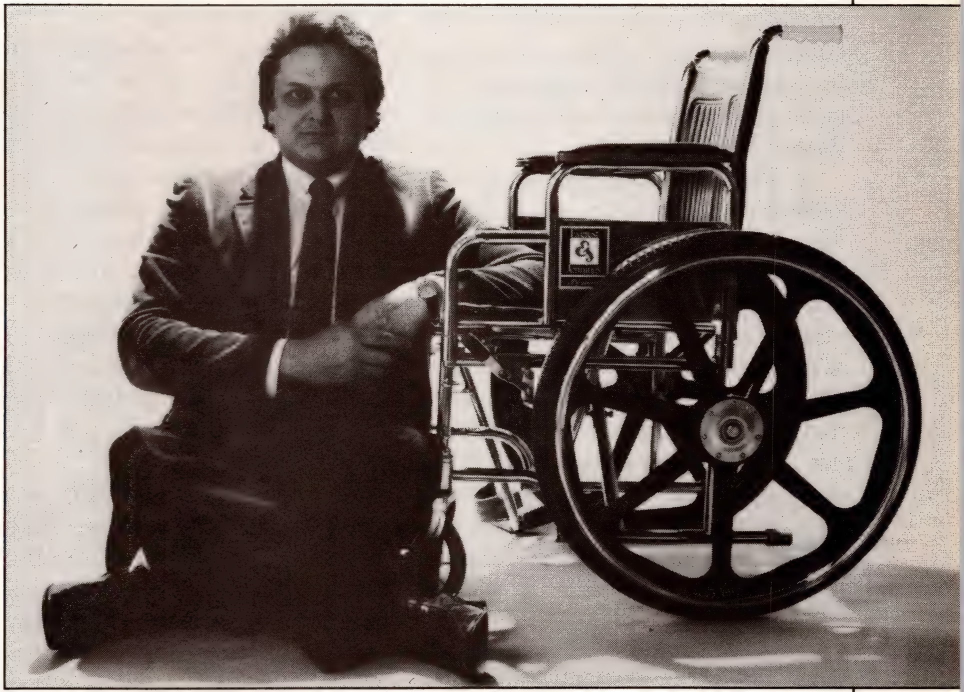
After high school, Arnold enrolled in the electrical-engineering program at the Case Institute of Technology (now Case Western Reserve University) in Cleveland, OH. A successful engineering career seemed imminent.

But after one semester at Case Insitute, Arnold left school and enlisted in the US Army. He flew more than 500 hours as a helicopter pilot in Vietnam. In 1970, while he was flying as copilot on a mission that took him 1½ hours west of Da Lat, his aircraft crashed. He suffered a broken back, and his legs remained paralyzed from the knees down. The injury derailed his educational and career plans.

> "I was getting tired of waiting for someone to find a cure for spinal-cord injury. I figured if they wouldn't do it, I'd try."

Now, at age 38, Arnold has returned to college to earn the degree he began studying for 20 years ago. A junior at the University of Akron, OH, he expects to complete his BSEE in two years and then pursue a master's degree in biomedical engineering. Having started a consulting practice four years ago that specializes in electronics aids for people with spinal-cord injuries, Arnold sees room for much improvement in the available technology. He hopes someday to close that gap. "People don't make electronic wheelchairs for the handicapped designed to MIL specs," he says. "People think that when they design for the handicapped, they can design at a minimal level. But the opposite is true, because if you don't operate a wheelchair deftly, you hit a lot of walls."

After completing his rehabilitation in the Veterans Administration Hospital at Wade Park (Cleveland, OH), Arnold spent several years trying out different jobs. He studied photography and opened a business as a children's photographer. Working with a friend, he produced jazz concerts and acquired public-relations expertise.



***Ralph Arnold**, consultant, Memories Unlimited Inc*

He also continued to pilot helicopters. After nine months of negotiations with the Veterans Administration, Arnold managed to convince the Administration to pay for his training as a civilian helicopter pilot through its vocational-rehabilitation program. Throughout the protracted procedure, Arnold contemplated why he was so driven to fly again. "It was what I was most familiar with, and what I was best at before the injury," he says of flying. "Yet sometimes I wondered if I really wanted to fly, or if it was a matter of getting back onto the horse that threw me off."

In 1972, he climbed back into the cockpit of a helicopter, and 250 flight hours later, he received certification as a civilian, commercial, and instructor pilot. He also earned a license to pilot a single-engine airplane.

Throughout all of his ventures, Arnold continued to tinker with hardware. "I put together all sorts of odd little circuits," he says. "By the mid 1970s, I could strip down most things and repair them. But I wasn't sure why they had been designed in a certain way." In 1978, he bought an Apple II+ computer and began teaching himself to program in Basic and assembly language. He enrolled in a class in Fortran at Kent State University.

In 1979, he attended a summer session in Blacksburg, VA, on interfacing to the 8080 Series chips. Though Arnold was primarily interested in the 6502 line, he found the class enormously informative. What's more important, it boosted his self-confidence. "When somebody first sits down with a chip, it's not like a fuse, which blows up if you do something wrong. This class gave me the confidence to put together some chips, even if it was something simple like a decade counter."

Meanwhile, his association with the Veterans Administration evolved into a consulting role. The hospital's vocational-rehabilitation program had purchased three Apple IIe computers, and Arnold drove to the VA hosital in Cleveland once a month to teach programming to residents. He'd also maintain the equipment, loading the hard disk, installing public-domain software, and hooking up peripherals.

In 1984, Arnold established Memories Unlimited, a consulting practice that specializes in troubleshooting electronic devices used by people with limited mobility and communications skills. Among his clients is a 36-year-old stroke victim with whom Arnold began working in 1986. "He lived as a vegetable in the VA hospital until they dicovered he was coherent," Arnold says. "Then it was a matter of interfacing him to the world." With Arnold's guidance, the man, who's paralyzed from the nose down, wears a light stick attached to eyeglass frames and uses the device to communicate on a computer, operate a modem, and write letters. Using slight head movements, he beams the light for a specified period of time at a photocell that illuminates a letter on the LCD in front of him.

Discovering the potential freedom that electronics holds for people with disabilities re-ignited Arnold's interest in an engineering career. It also persuaded him to resume his formal engineering education—despite some qualms about attending classes full of 19- and 20-year-olds. Arnold happily reports that, because the University of Akron is a popular choice for other nontraditional students like himself, he's not the oldest student in any of his classes.

He applies to his full-time undergraduate studies the same diligence he's shown in a lifetime of self-education. "I look at electronics as being the tool that will someday let me hook patients up to a machine with which they can run anything they want," says Arnold. "I was getting tired of waiting for someone to find a cure for spinal-cord injury. I figured if they wouldn't do it, I'd try."

Bob Barnes' electrical-engineering education began at the age of three, when he stuck his finger into a light socket. "I started asking questions then," he remembers. "Every answer led to another question, and I've never stopped asking questions since."

The answers to Barnes' questions propelled him along the way to an engineering career. In high school, he was a frequent Radio Shack customer and a fan of the chain's 151-projects kits. He later studied electrical engineering at Louisiana Tech University, and after graduation in 1979 he delayed his full-time job search by several months to pursue the art of television repair. "A television contains an example of nearly every kind of circuit there is in electronics. And that can't be said of any other device. The most sophisticated computer in the world contains hundreds of thousands of repetitions of the same circuits."

"Blind people are 85% unemployed or underemployed. The computer is the ticket in for them."

For the past eight years, Barnes, 31, has worked for General Dynamics in Fort Worth, TX. Now an engineering specialist, he programs automatic test equipment (ATE) in the department of manufacturing-test-equipment engineering. After several years of programming, he's now training newcomers to his department in the techniques used to test avionics equipment both on the production line and in the field.

Barnes has been blind since birth, and he says his presence in the engineering laboratory sometimes surprises first-time visitors. "When people come into the lab with a technical question and they're referred to me, they don't realize I'm blind until they reach my desk. That surprises people, and they don't know how to go ahead and ask their question. They usually have a drawing that illustrates some of their problems and now they have to describe it." Yet Barnes understands their hesitation. "It's a cautiousness around situations they're unfamiliar with."

Among the engineers with whom he works, however, Barnes says such initial awkwardness quickly evaporates. "A lot of people view blindness as a barrier to be avoided. But the people I work with view it as a challenge to be overcome so that they can use the abilities a person has." The only special equipment Barnes uses is the computer system that he works with daily. It employs a braille keyboard and a terminal that displays one line of 20 braille characters. A nearby printer produces Barnes' program listings in braille.

Indeed, Barnes sees computer training as a great asset to people in all levels of the workforce who have limited sight or no sight. "Blind people are 85% unemployed or underemployed. The computer is the ticket in for them. There are many noncomputerized offices where able-bodied people are somewhat afraid of computers. They can afford that fear because they are getting by. Blind people can't afford to be afraid."

Even with job applicants that have the appropriate skills, however, it's often difficult to convince people in the workplace to look beyond physical limitations. Corporate recruiters, for example, can become preoccupied with what a person can't do. Often they ask interviewees how they will handle the physical aspects of getting around in the office and the paperwork associated with a position. Such questions are legitimate, Barnes points out, but difficult to answer at an interview, when the job candidate knows little about the physical characteristics of the building or the acceptability of asking others for assistance with paperwork.

More important, the applicant has undoubtedly tackled such logistical problems before and will be able to do so again. Barnes says that he had a ready answer for recruiters who asked him the inevitable questions. "I made it quite clear that these are the kinds of problems I've solved all of my life." Good salesmanship became an important part of his pitch. "Even if employers believe you, they consider themselves going out on a limb. They have to be sure."

Barnes serves as chairman of the board of the Center for Computer Assistance to the Disabled in the Dallas-Fort Worth area. Local residents and businesses provide the financial support and equipment

© Jay Elledge/Farrington

Bob Barnes*, engineering specialist, General Dynamics* that Barnes and others use to teach computer skills to area residents who are blind. Barnes hopes the training will be the catalyst the center's clients need to start down the road to success.

William Ganey recently retired after a 36-year engineering career. He began his career in 1951, designing command, control, and communication electronics for the Nautilus atomic submarine. After working on simulation and training for aircraft radar operators, he eventually participated in the Titan, Minuteman, and Peacekeeper missile projects. He also worked on a project that examined the feasibility of supporting a moon-based military and scientific station.

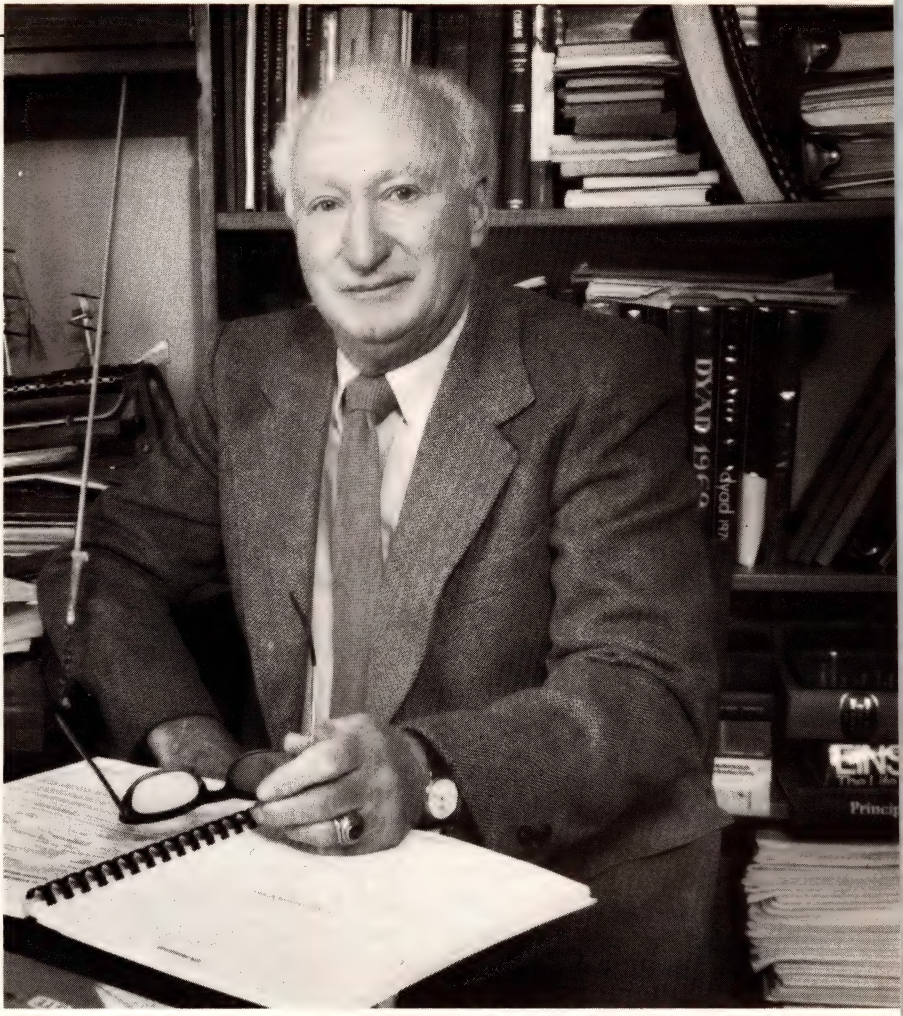
For the last 27 years, Ganey worked for GTE's Strategic Systems Div in Westborough, MA. In October 1987, he retired as engineering manager in the company's independent research and development laboratory.

He sustained nerve damage to both ears during World War II, when the Japanese blew up the island he had just landed on as a paratrooper. He retains 30% of his hearing.

Ganey never considered his limited hearing a hindrance: In addition to being a good engineer, he considers himself a good salesman. He simply sharpened his skills in self-promotion. "I was able to sell myself, which is something everyone has to do," he says. "Once I got into the engineering department, I had no trouble."

When talking with other engineers, he would position himself directly in front of them in order to facilitate lip-reading. But he did encounter difficulty in corporate personnel departments. "Personnel tends to look down on people with disabilities. If two people vying for a job have equal capabilities, the job generally goes to the person without the disability."

Martha Everson



William Ganey, *retired engineering manager*

For Ganey, the after-hours aspect of business sometimes posed a problem. "Lots of business is actually conducted outside the workplace—in restaurants, for example," he says. Though he usually has few problems when he wears a hearing aid in each ear and reads lips, noisy, crowded rooms are a challenge. The human ear adjusts and compensates for each environment, but mechanical hearing aids don't have that ability. When a person wearing a hearing aid enters a clamorous room, his ears are bombarded by loud, painful sounds. Many people turn off their hearing aids in such situations, relying on their lip-reading skills and sometimes feeling isolated. "A lot of people fake it. They nod and try to stay part of things," Ganey says.

"With a hearing loss, lots of people become introverts, and they miss an awful lot of life," says Ganey, who is 64. Ganey worked hard to avoid such seclusion. At one point in his career, he simultaneously managed engineering projects in Massachusetts, California, and Colorado. He spent 50% of his time traveling, and he made an effort to dine in restaurants with his business-trip colleagues and to attend corporate and social functions despite the discomfort he sometimes felt. "I couldn't avoid [the socializing]," he says. "It was the most difficult part of my job."

When GTE won a $500 million contract to develop the MX missile, the company threw an elaborate celebration party. The din created by 2000 guests made for a difficult evening not only for Ganey, but also for other attendees. His boss later pulled him aside and asked him if he'd had trouble hearing at the party. When Ganey answered yes, his boss commented that he, too, had had trouble hearing. The experience, his supervisor said, gave him a better understanding of Ganey's difficulties in public places.

"I want to use the benefit of my experience to help someone who's just starting out."

Ganey found his hearing impairment a small obstacle compared with the hurdles faced by individuals who need—and usually don't receive—more support from the workplace. For example, another engineer Ganey worked with had limited use of his legs and walked with the assistance of crutches. The two men frequently traveled together and Ganey often had to watch his colleague struggle with long flights of steps in facilities that had no elevators. "Industry doesn't do anything for handicapped people unless they're forced to by the government," he laments. "They put in ramps and special parking spots, but that's about as far as they go."

Since his retirement last fall, Ganey's decided to devote more of his time to providing guidance for young people with disabilities. He's a member of the Project on Science, Technology, and Disability within the American Association for the Advancement of Science, and he's listed in the Project's *Resource Directory of Scientists and Engineers with Disabilities*. Says Ganey: "I want to use the benefit of my experience to help someone who's just starting out." **EDN**

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3/22 Tuesday	9:00-11:00 AM	UNISYS CORPORATION Township Line & Union Meeting, Blue Bell, PA
3/22 Tuesday	11:30-1:00 AM-PM	KULICKE & SOFFA INDUSTRIES, INC. 2101 Blair Mill Road, Willow Grove, PA
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4/14 Thursday	2:00-4:00 PM	WANG LABORATORIES, INCORPORATED One Industrial Ave., Lowell, MA
4/15 Friday	8:30-10:00 AM	DIGITAL EQUIPMENT CORPORATION 295 Foster St., Littleton, MA
4/15 Friday	11:00-1:00 AM-PM	DIGITAL EQUIPMENT CORPORATION 146 Main St., Maynard, MA
4/15 Friday	2:00-4:00 PM	DIGITAL EQUIPMENT CORPORATION 200 Forest St., Marlboro, MA
4/18 Monday	9:00-11:30 AM	DATA GENERAL CORPORATION 4400 Computer Dr., Westborough, MA
4/18 Monday	1:00-4:00 PM	DIGITAL EQUIPMENT CORPORATION 333 South St., Shrewsbury, MA
4/19 Tuesday	8:00-10:30 AM	IBM CORPORATION Neighborhood Rd., Kingston, NY
4/19 Tuesday	11:30-1:00 AM-PM	IBM CORPORATION South Rd., Poughkeepsie, NY
4/19 Tuesday	2:00-4:00 PM	IBM CORPORATION E. Fishkill Rd., Hopewell Jct., NY
4/20 Wednesday	9:00-12:00 AM-PM	IBM CORPORATION Bodle Hill Rd., Owego, NY
4/20 Wednesday	1:30-4:00 PM	IBM CORPORATION Glendale Dr., Endicott, NY
4/21 Thursday	8:30-10:30 AM	GENERAL ELECTRIC COMPANY Broad St., Utica, NY
4/21 Thursday	11:00-12:00 AM-PM	GENERAL ELECTRIC COMPANY French Rd., Utica, NY
4/21 Thursday	2:00-4:00 PM	GENERAL ELECTRIC COMPANY Farrell Rd., Syracuse, NY
4/22 Friday	8:00-10:00 AM	XEROX CORPORATION 800 Phillips Rd., Webster, NY
4/22 Friday	10:30-1:00 AM-PM	EASTMAN KODAK COMPANY 901 Elmgrove Rd., Rochester, NY
4/22 Friday	2:00-4:00 PM	HARRIS RF COMMUNICATIONS 1680 University Ave., Rochester, NY

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Responsible for managing the software and systems design of all workstation products. You will also provide technical and administrative management services with regard to both hardware and software engineers. Requires knowledge of 'C', FORTRAN, UNIX, GKS, PHIGS, and Graphics with a minimum of 7 years relevant experience.

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You'll become part of a group responsible for the development of drivers and software interfaces for industry standards on both raster and vector refresh graphics systems. Knowledge of UNIX, VMS, FORTRAN 77, 'C', opsystem driver design, Assembly language, PHIGS, and GKS, plus graphics experience are desired. In addition, we're looking for approximately 5 years relevant experience.

HARDWARE ENGINEER—RASTER

A key contributor to the group responsible for the development of new graphics products is needed. Knowledge of bipolar, CMOS technology, graphics, some bit slice firmware, and familiarity with graphics algorithms are required. You should also possess approximately 5 years relevant experience to make the level of contribution desired.

RELIABILITY/MAINTAINABILITY ENGINEER

Responsible for all aspects of reliability and maintainability programs including proposals, administration, field failure analysis and customer interface as required. Requires 2-5 years experience in reliability and maintainability programs, analysis and calculations such as MTBF. Good verbal and written communication skills.

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EDN

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Apr. 14	Mar. 23	Communication Technology Special Issue, Communication Systems	Closing: Mar. 31 Mailing: Apr. 21
Apr. 28	Apr. 7	Software, Industrial Computers, Interface ICs	
May 12	Apr. 21	Analog Technology Special Issue, Analog Converters	Closing: Apr. 28 Mailing: May 19
May 26	May 5	CAE, Software, Sensors/Transducers	
June 9	May 19	CAE, Analog ICs, Test & Measurement	Closing: May 29 Mailing: June 16
June 23	June 2	Data Communications, DSP, Components	
July 7	June 14	Product Showcase—Vol. I, Power Sources, Software	Closing: June 23 Mailing: July 14
July 21	June 30	Product Showcase—Vol. II, CAE, Test & Measurement	
Aug. 4	July 14	Sensors & Transducers, Analog ICs, Graphics	Closing: July 21 Mailing: Aug. 11
Aug. 18	July 28	Military Electronics Special Issue, Displays, Military ICs	
Sept. 1	Aug. 11	Instruments, Op Amps, Computers & Peripherals	
Sept. 15	Aug. 25	Data Acquisition, Data Communications, Digital ICs	Closing: Sept. 1 Mailing: Sept. 22
Sept. 29	Sept. 8	DSP, Grahics, Optoelectronics	
Oct. 13	Sept. 22	Test & Measurement Special Issue, Instruments, Computers & Peripherals	Closing: Sept. 29 Mailing: Oct. 20
Oct. 27	Oct. 6	CAE, Computers & Peripherals, Integrated Circuits, Wescon '88 Show Preview	
Nov. 10	Oct. 20	Programmable Logic Devices, Integrated Circuits, Test & Measurements, Wescon '88 Show Issue	Closing: Oct. 27 Mailing: Nov. 17
Nov. 24	Nov. 3	Microprocessor Technology Directory Graphics, CAE	
Dec. 8	Nov. 16	Product Showcase—Vol. I, Power Sources, Software	Closing: Nov. 21 Mailing: Dec. 15
Dec. 22	Dec. 1	Product Showcase—Vol. II, Computers & Peripherals, Test & Measurement	

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- Configuration Management in accordance with MIL-S-483

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Manage hardware and software diagnostic testing with state-of-the-art automatic test equipment. Your BSEE or MSEE degree should be complemented with at least two years' related experience in designated ATE test fixtures/bed of nails fixtures with a background in power supply testing and transmission line theory as related to fixturing.

Familiarity with Teradyne L200 and Genrad test equipment, "C" and Assembly programming languages, using industry standard architecture and MS-DOS in an 80286/80386/8086 environment is essential.

Component Test Engineers:

You'll ensure quality control through engineering analysis, device characterization, and failure verification of digital and linear devices such as: custom ASICs, complex microprocessors and periphera advanced CMOS logic, static and dynam memories, and other precision componen

You should have a BSEE and three years' experience in either ATE compone test equipment, analog testing, printed circuit boards, component/incircuit boards, or vendor quality inspection and supplier selection.

Vendor Quality Engineers:

Coordinate device qualifications with vendors and purchasing. You'll lead the way conducting tests and evaluating desi and redesign peripheral problems to ma tain the highest user satisfaction ratings through quality control. You must have a least two years' experience with peripher and project management, plus a BSIE or BSEE degree.

Cost Reduction Engineers:

Provide innovative solutions to cost reduction problems by creating designs to meet the requirements of established goals. You should have a BS in EE, EET,

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Provide direct packaging engineering support for manufacturing operations, as well as product development support through improved packaging designs. Your BS in ME, Packaging Engineering, or equivalent, plus three years' related experience qualifies you for this challenging position. Excellent interpersonal skills are required to develop strong working relationships with outside vendors, contractors and consultants, as well as with multiple internal organizations.

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Challenge your expertise in high-speed logic design and/or microprocessor system design using flow charts and timing diagrams for digital design and detailed design analysis. Your experience should include vendor libraries, test vector generation, simulation checkout, and TTL emulators for gate/array standard cell design. Familiarity with CAE systems used in logic design, test vector generation, simulation checkout, and documentation is also necessary. You must have five years' related experience plus a BSEE or equivalent degree; an MSEE degree is preferred.

Systems Software Engineers:

Evaluate, design, and develop firmware, operating systems, device drivers, and utility software for PC systems. You'll need a BSCS, BSEE or equivalent degree with four years' related experience in PC software development, 8086/286/386 Assembly/''C'' language programming in MS-DOS, OS/2, and/or UNIX/XENIX operating systems.

Systems Architects:

Design new products by investigating and evaluating system compatibility and performance of design alternatives and new technologies. You'll develop hardware compatibility tests and performance analysis tools.

Qualify with a BSEE, MSEE preferred, and three years' hardware background with a knowledge of microprocessor-based systems software. In addition, experience with CPUs/memory/bus architecture, numeric co-processors, file subsystems, network/communications, graphic subsystems, and state machines is required.

Graphics Display Manager:

Coordinate and manage the definition, development and procurement of display subsystems. You'll provide compatible systems and develop high resolution products for engineering workstations, desktop publishing, and related applications.

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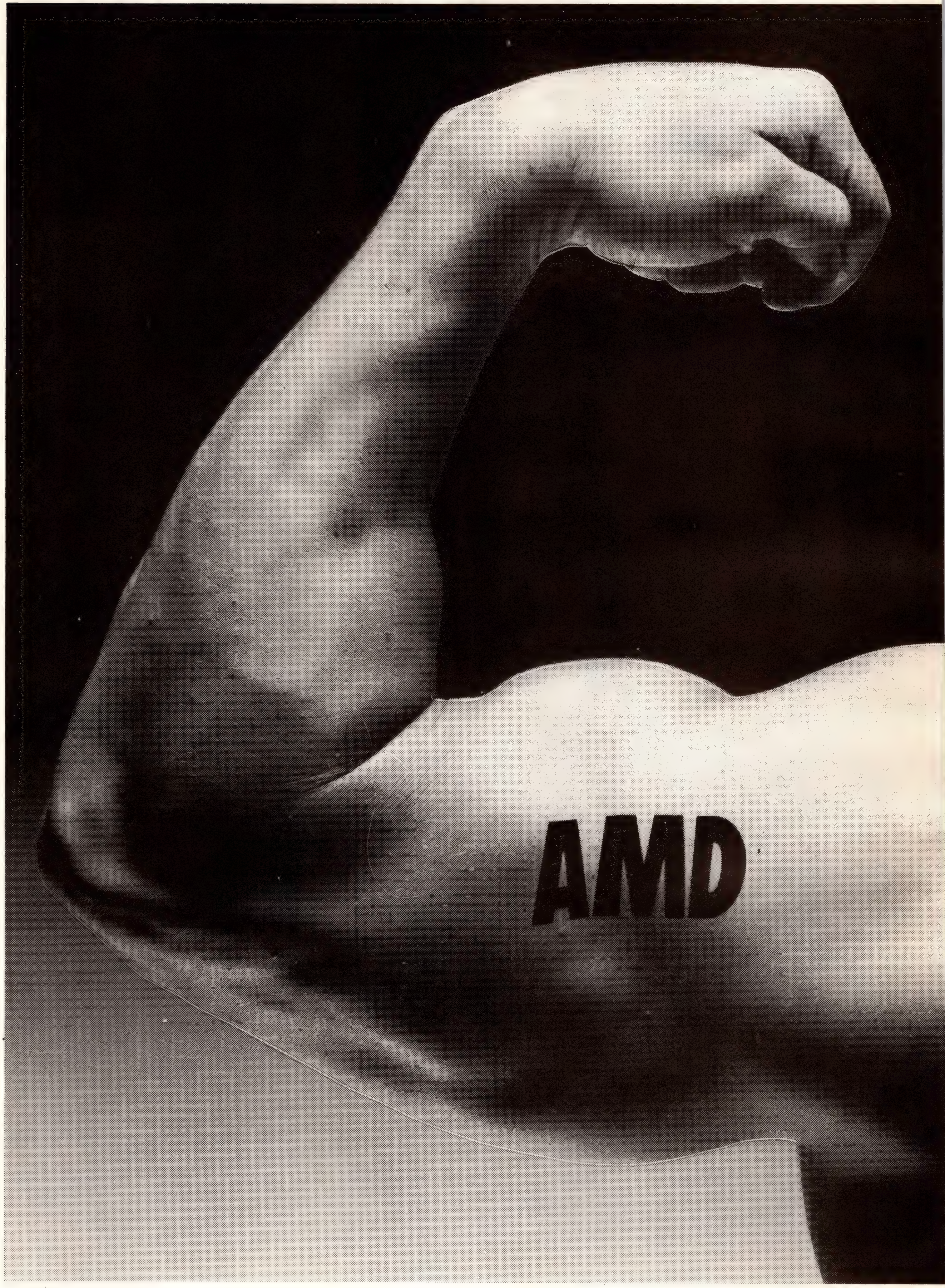
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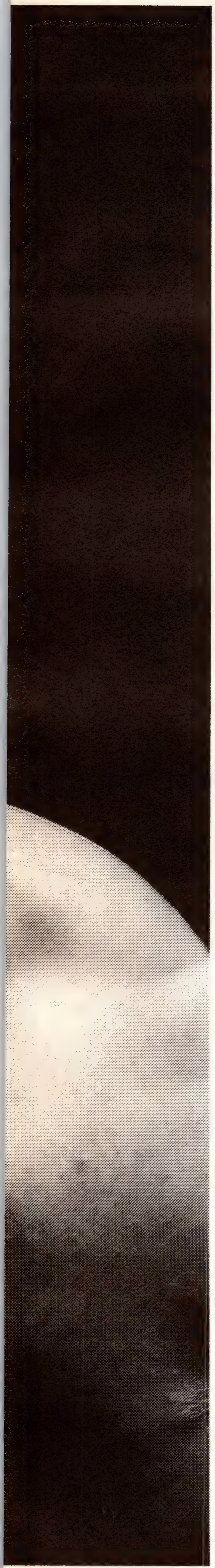

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- **Applications**
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- **Technical Publications**

For information about Texas opportunities, call Richard Holtry at (512) 462-5470, or send your resume to him at Advanced Micro Devices, MS-525, 5204 East Ben White Blvd., Austin, Texas 78741.

For information about California opportunities, call Mike Gore at (408) 749-5555, or send your resume to him at Advanced Micro Devices, MS-57, 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088. An equal opportunity employer.

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- **Operating Systems (UNIX, VAX/VMS, RSX11M, RMX86).**

HARDWARE DESIGN ENGINEERS

Requires extensive experience in:

- **Digital Logic Circuit Design, ASICS, MOS, CMOS, ECL, TTL, PLD's**
- **Motorola Micros (68000/20), Intel Micros**

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Requires extensive experience in:

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- **Hardware & software systems**

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State of the art project on the PDP 11 running RSX11M. Requires extensive experience in:

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- **Microprocessors, minicomputers, DEC computer systems**

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Requires an Associate's Degree (or equivalent) and 4 years extensive experience in:

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This position requires a minimum 10 years' experience in software development, software configuration management and software audit. Familiarity with DOD-STD 1679 is essential.

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Qualified individuals must have at least 2 years' experience in one or more of the following:

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- TACPOL
- MOL (ASSEMBLER)
- NICS-TARE Systems
- CHRISTIAN ROVSING CR-80 computer

Teaching experience or 3 years' in telecommunications programming along with system programming experience are preferred.

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We are seeking a Sr. Quality Engineer with a minimum of 5 years recent experience in a military electronics industry to perform primary interface with program office, subcontracts and engineering. Will obtain, and analyze quality and inspection requirements for TAOC/MCE and ships programs subcontracts and set up inspection plans and hiring schedules to support subcontract build and delivery schedules. Extensive travel is required.

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Will be responsible for subcontractor evaluation controls to MIL-Q-9858 and MIL-STD-1535A. Requires a CQE with a BS in Engineering and 3-5 years' experience in Supplier Q.E. and Production Q.E. of government electronics equipment, i.e. circuit board assemblies, power supplies.

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You will use your extensive engineering background to expand the electronic design standards and technology function in accordance with DoD Directive 4245.7M (Transition to Production) and NAVSO P.6071 (Best Practices). The successful candidate will possess a minimum 15 years' technical hands-on experience. Requires a BSEE (advanced degree desirable) and a working knowledge of digital and analog design, component technology and specifications, testability requirements and management techniques.

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Will work on division A.T.E. in Software development for unit level testers. Microprocessor Hardware design experience and familiarity with CMS2 programming language desirable. Requires 3-5 years' experience, BSCS/BSEE and the ability to follow a project through design, development and integration.

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Due to a recently received major DoD multi-year production contract for mobile, modular C^3I Air Defense Systems for Air Force and Marine Corps, we need strong systems engineers with a BSEE (Master's preferred) and 10 or more years experience to develop international applications of these systems for tactical air operations. In addition, concepts for product improvement are needed for existing system configurations. Immediate openings exist for motivated, experienced systems engineers to lead the Engineering design process by performing requirements analyses, functional syntheses and hardware/software trade studies in the following areas:

- Tactical Air Operations
- Direct Air Support
- Command Operations Centers
- Forward Area Air Defense
- Artillery Fire Support
- Sensor Fusion
- Data Link Integration

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- Requires a Sr. Software Engineer with experience on large military command and control systems. A background in CMS2 language and experience with communication data links such as TADIL-A, TADIL-B, TADIL-J, LINK-1 and ATDL-1 are highly desirable.
- Requires 5-10 years' experience in Assembly language programming for military systems and a minimum 5 years' experience in digital signal processing applications.
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Above positions require a BS in Computer Science or Engineering.

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- Will generate PDL from detailed design documents, coding of programs in CMS2 and Assembly language and unit testing of the programs. Requires 3-8 years' software experience.

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EDITED BY CYNTHIA B RETTIG

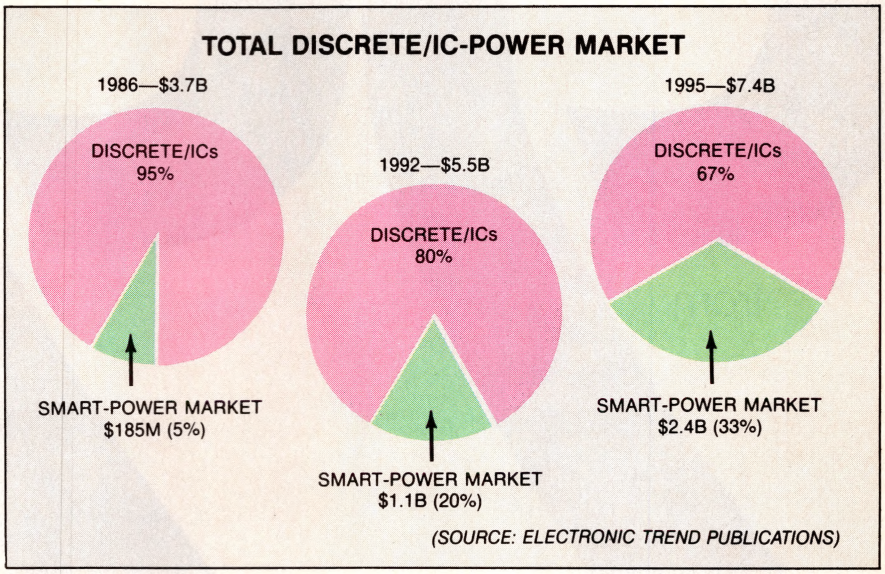
Smart power invades IC/discrete-device market

The practice of combining logic with power-control functions to produce smart power devices will "revolutionize" electronic-component design within the next few years. According to Electronic Trend Publications (Saratoga, CA), the worldwide market for smart power devices of more than 2W should attain a value of $1.1 billion by 1992, largely as a result of automotive, consumer, office-automation, and commercial- and military-aircraft applications. Indeed, by 1995, such devices will claim 33% of the total IC and discrete-product market, accounting for $2.4 billion in sales.

Traditional power supplies can occupy as much as one-third of equipment space. Thus, replacing numerous discrete components with fewer chips—or, in some cases, with a single, monolithic chip—lowers both component count and system costs. Smart power devices also improve system reliability.

For example, smart-power ICs can improve individual features, overall performance, and reliability in the motion control of stepper and brushless dc motors. Other major areas of application include programmable voltage regulators and ignition controllers.

Manufacturers are currently employing various processes in the fabrication of smart-power ICs. The application of VLSI technologies, especially MOS, to power-control devices constitutes a major trend. However, some IC vendors are employing bipolar and MOS technologies to make multichip or hybrid designs that are geared toward improving specific device applications and performance. Furthermore, custom ICs should continue to play a significant role in the smart-power market through the mid-1990s.



(SOURCE: ELECTRONIC TREND PUBLICATIONS)

ETP predicts that a variety of high-voltage monolithic ICs will streamline design problems by rendering obsolete those hybrid circuits that require large numbers of components. These monolithic ICs will incorporate various technologies including bipolar, DMOS, and CMOS, or combinations thereof. When higher voltage is required, hybrid and multichip solutions will fill the bill.

Because the successful combination of logic and power functions obviously remains central to the future of smart power devices, some companies are forming strategic alliances in an attempt to get dependable products to the market as quickly as possible.

Changes forecast for electronic car sensors

The 1988 market for electronic, electromechanical, and electrical automotive sensors will have a value of nearly $2.7 billion. By 1992, the market's value will increase to $3.8 billion, representing an annual growth rate of 9.2%, according to a recent study conducted by Venture Development Corp of Natick, MA. However, it remains to be seen whether consumers will be willing to pay the added costs resulting from the inclusion of sensors in automobiles.

Automotive sensors detect physical parameters and convert them into measurable signals that various types of controllers can then use to make adjustments. These parameters include pressure, temperature, speed, position, oxygen content, vibration, motion, and acceleration. In US-built passenger cars, temperature, position, pressure, oxygen content, and speed currently comprise the bulk of applications. However, there will be increasing demand for applications involving such parameters as torque, motion, vibration, proximity, instrumentation, and other vehicle-control mechanisms.

Traditionally, automotive sensors have employed electrical/electromechanical technology. Now, however, auto manufacturers are beginning to install sensors that use ICs capable of performing simple logic functions. Moreover, truly smart electronic sensors—that is, sensors that employ µP technology—should become available in the early 1990s.

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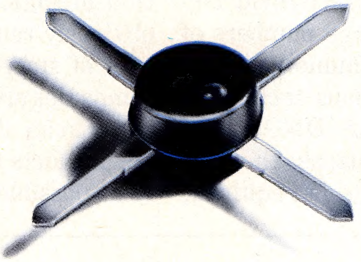

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MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
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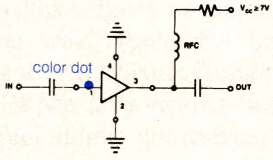

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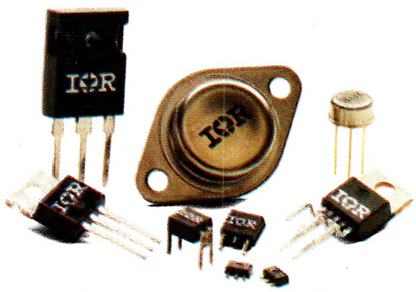

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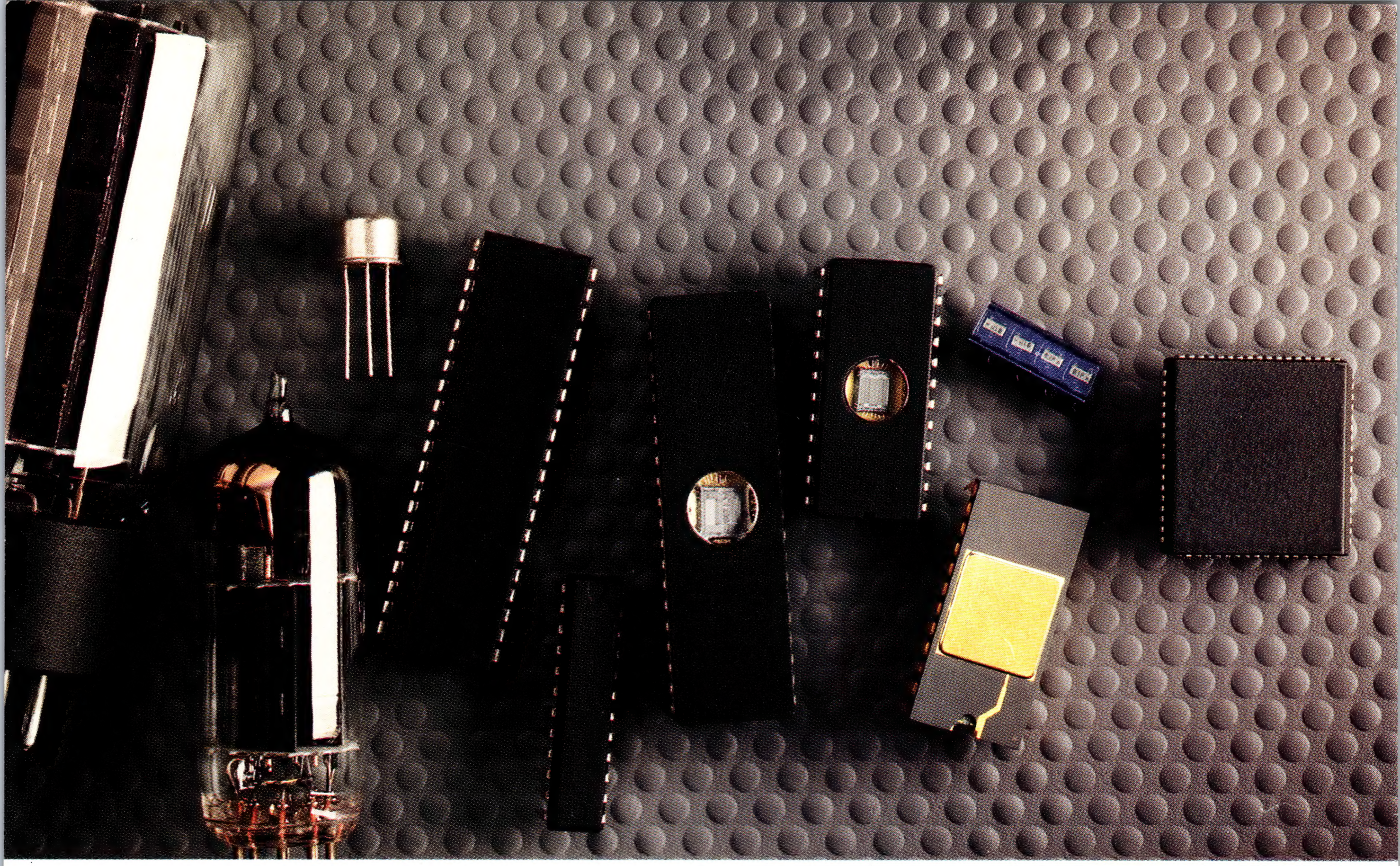

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